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Tactical Exploration of Single Electronics Simulators for the Designing of nm Device Architectures

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ABSTRACT: Single Electronics research encapsulates two successive methodologies - Single Electronics fabrication including its physical realization and soft computation of Single Electron made circuits and its logical interventions. Fabrication oriented research augmented largely in the last two decades but the later form of research is tailing quite far. Although, manifestation of a limited number of user friendly software for Single Electronics modelling is availed but a cognitive study of these software is obligatory. The authors here combine few of these popular software based on their designing criterion. The aim is to have an ample insight into the legitimacy of these simulators in modelling Single Electronics based device architectures.

Keywords - Singe Electronics, Master Equation, Monte Carlo, Macro-Modeling, Simulators

I. INTRODUCTION

Feature size reduction is one of the critical elements in today's fabrication technology. In 2003, International Technology Road Map for Semiconductors (ITRS) [1] vindicated the upcoming of several new topologies beyond CMOS to pave the new horizon of technological shift due to the urge of size reduction. This technological shift is attributed as driving force of today's Nano electronics which is governed by 'freedom electronics'. In this regard analytical studies have geared up and are now modernizing itself to catch up with the present eco-socio trend.

The three new topologies that ushered numerous research initiatives are Quantum Electronics (QE) [2 & 3], Single Electronics (SE) [4-7] & Spintronics [8-13]. Besides, the other few dominating candidates in this category are Resonant Tunneling Diodes (RTD)s [14-16],Rapid Single Flux Quantum (RFSQ) devices [17],Quantum Tunneling Diodes (QTD)s [18] etc. Here in this communication, the Researchers bind themselves within the three former topologies. On the other hand QE is facing tremendous challenges owing to its inherent physical limitations [19 & 20] & Spintronics based analysis is in its embryonic stage.

Device Researchers pioneered in fabrication topology of these devices from its very inception. The present available fine line lithography techniques for fabrication are significantly time consuming and definitely they are very costly, even though worldwide government organization invests whole heartedly in these critical researches and contribute largely. This has augmented the fundamental fabrication oriented device research. Later on they tend towards conceiving typical analytical tools for more deliberate and higher accuracy in design specs. The soft computational aspects of device research fascinated Researchers in the last few years - it attracted thousands of Researchers worldwide. In particular, Researchers opted sophisticated computer oriented designing and modelling techniques to craft logic synthesis of SET using these tools. These are popularly attributed as soft computing tools. These tools are intrinsically

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blessed with vivid functionalities, accuracy, tolerance, time bound reflections and facilitate greater flexibilities to the users and to the device engineers. Thus the authors intend to limit themselves within the boundaries of Single Electron Transistors (SET) analysis using soft computing tools only.

II. MODELING AND SIMULATION OF SETs

The stipulated rise in the development of SE is likely to revolutionize microelectronic industry by the end of this decade [21-23]. This has motivated SET Researchers to involve more and more in the new generation of circuit architecture designing. Consequently, the modeling techniques and simulation frameworks of these SET based devices has geared up. In terms of modeling the SET logic devices, numerous research attempts have been reported [24-27]. To cognize the performance of SET logic circuit three 'M' methodologies are considered for simulation - Master Equation (ME), Monte Carlo (MC) and Macro-Modeling (MM) method. Apparently Analytical Method is another substantial element in this category. Few such models are semi classical in nature [28].

III. ME BASED SET MODELLING

SE properties are keenly observed in ultra-small dimensional devices and the same was first empirically demonstrated by Likharev in 1999 [29]. Often they are pragmatic for numerous novel types of logic and memory circuitry. Most SETs are based on the Orthodox Theory [30] of the SE. As numerical simulation of the SET helps a great deal in analyzing the effectual tunneling and co-tunneling phenomena, ME based simulators are deliberately considered to simulate numerically V-I characteristics of SETs. It eventually adheres to the Markov process of electron tunneling [31], and it mimics the exact mathematical model for the electron tunneling events. Thus ME is entitled both for static/dynamic characteristics widely.ME simulation technique for SET is based on the probability distribution of electrons which is coupled in the SET quantum structure and it is attained using stochastic process. It facilitates the control of device characteristics. Ratno Nuryadi an eminent Researcher in SET corroborated the ME technique to resolve electron tunneling probability in SET dot [32]. The steady state ME and the current calculation is obtained by equation (i) to (iv) including the tunneling probability. Free Energy $Q_{1\&2}$ is derived from [32].

$$P_1^{\pm}(M) = \frac{1}{N_1 C^2}\left[\frac{-\Delta Q_1^{\pm}}{1-\exp\left(\frac{\Delta Q_1^{\pm}}{H_E J}\right)}\right] \quad \text{.....(i)}$$

$$P_2^{\pm}(M) = \frac{1}{N_b C^2}\left[\frac{-\Delta Q_2^{\pm}}{1-\exp\left(\frac{\Delta Q_2^{\pm}}{H_E J}\right)}\right] \quad \text{.....(ii)}$$

The Steady State ME is derived from

$$\sigma(M)[P_2^{-}(M) + P_1^{+}(M)] = \sigma(M+1)[P_2^{+}(M+1) + P_1^{-}(M+1)] \quad \text{.....(iii)}$$

Thus the Current Equation happens to be-

$$S(E) = c\sum_{M=-\infty}^{\infty}\sigma(M)[P_1^{+}(M) - P_1^{-}(M)] = c\sum_{M=-\infty}^{\infty}\sigma(M)[P_2^{+}(M) - P_2^{-}(M)] \quad \text{....(iv)}$$

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In the above equations the following parameters are treated as follows - P_1 =Tunneling probability rate, M= the number of electrons in dot, N_1,N_b =Tunnel Resistors, C=Elemental charge, ΔQ=Energy change, H_E=Boltzmann Constant, J=Temperature.

But the fragility is that it is operative merely for simple circuits which have few islands [33]. Other apathetic demerit is that it cannot explore the dynamics of the microscopic tunneling events in SETs as it deals only with average values [28]. A MATLAB implementation of the ME is also proposed in [32]. Few revolutionary simulants applying ME are SENECA by Fonseca et al. [34] and SETTRAN by Korotkov [29].

IV. MC BASED SET MODELLING

Quantum Mechanics although imperative in device throughput yet it only calculates the probability of any outcome; to the contrary MC uses a random number stochastic nature of charge based technique and is a more appropriate technique to simulate quantum systems as opined by Wang Sheng [35]. MC gained much popularity as it simulates the electron tunneling events robustly so that actual tunneling occurrences in SET circuits can be directly emulated. In transient simulation, it is assumed that tunneling events occur instantaneously. A simplistic view on MC can be obtained by introducing Tunneling rate (T_c) in equation (v) for the P- probability that tunneling will occur in t-time duration.

The probability for the tunneling occurrence in n sec(s) is provided by -

$$P(n) = 1 - \exp(-\mathrm{Tn}) \quad \text{.....(v)}$$

Therefore, time to the tunneling event is determined as

$$\Delta n = -\frac{1}{T_C}\ln(1-q) \quad \text{.....(vi)}$$

Here, T_c=Tunneling rate, P=Probability that tunneling occur in n seconds and q=Random Number.

It assembles all probable tunneling events, computes their probabilities and randomly chooses one of the possible tunneling events based on the weighted factors. To acquire the desired electron transport phenomena in the circuit hit-and–trial process is initiated. The tunneling events are not only independent abut are robust and exponentially distributed in nature. Eminent Researchers Amiza Rasmi and Uda Hashim elucidated the MC process in [30]. The MC method is extensively prevalent in MOSES simulation tool designed by Chen et al. [36] and SIMON simulator by Wasshuber [37].

V. MM BASED SET MODELLING

The Macro-Modeling method ponder over the macro-characteristics of electron tunneling that expedite SET circuit simulation using CAD tools with utmost efficiency for large circuits. Thus, the past few years envisaged stipulated rise in MM simulation of SET circuits. It is comparatively more trustworthy as it does not require any specific model [38] and turnstiles [39]. Due to its easy availability many existing models can be incorporated with certain secondary

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effects including background charge and temperature effects.MM is considered one as of the conventional circuit modeling techniques since it has unanimously modelled CMOS circuit designs from early '90s. Two classical assumptions are assimilated to design the MM of SET's. The primary assumptions are that once the parameter of the isolated transistor is determined from the device simulator and/or from any other modeling tools, the same can be incorporated to model the new circuit. Another assumptions is that the V-I characteristics of the device are driven by neighboring transistors only. The interactions between adjacent devices are marginalized .But the empirical study revealed that second assumptions for SET is simply unrealistic and thus can be neglected. Other dominating features include the effective charging of the Coulomb Island of SET which will be largely reciprocated in the neighboring islands of the other SET. It was introduced by Yu et.al. [40] and the parameters can be extracted from the following equations.

$$Q_1(E_G) = P_{N1} + P_{N2}\cos(P_{L1}.E_G) \quad \text{(vii)\&}$$

$$Q_2\,(E_{GS},E_{DS}) = Q_3\,(E_{GS,},E_{DS}) = \frac{PE_L}{PJ_2 - \frac{2PE_L}{Q_1(E_{GS},E_{DS})}} \quad \text{(viii)}$$

Q_1,$Q_2$and Q_3 are the resistors, E_G is the gate voltage, E_{DS} is the drain to source voltage, parameters P_{N1},P_{N2},P_{L1},PE_L,P_{J2},are used to fit the characteristics at various gate biases.MM based SET modelling is fully compatible to SMART SPICE and this has been revealed in the research work of Yu et.al.,(1998) [40], Wu-Line (2003) [41] and Mohammad Reza Karmanian (2010) [42]; they successfully validated SET SPICE modelling using MM techniques in the last decade.

VI. A GLIMPSE OF THE SOFTWARE USED FOR SET SIMULATION

Few remarkable software based upon MC/ME/MM used in SE computing research are- i)SIMON2.0 ii)MOSES iii)KOSEC iv)SMART SPICE v)BSIM 4.0. The authors in ephemeral put forward a speculative view in assessing the impetus of these tools in designing nm regime SET devices.

SIMON 2.0:-SIMON, a MC simulator for SET circuits provide graphical user interface and graphical circuit editor for smart usability. Numerous circuit elements including Tunnel Junctions, Capacitors, Voltage Sources and Measuring Devices for Current, Voltage, & Charge, can be called into the editor window using drag-drop method to obtain transient and stationary simulation of arbitrary SET circuits [37].Consecutive research attempts have been reported so far – few noteworthy research articles are cited here for perusal [37, 43-47].

Researcher	SIMON.2 Simulated Design	Year
C. Wasshuber	Single-Electron Tunnel Devices and Circuits	1997
J. Gope	SET based ASIC	2007
P.C.Pradhan	SR, D and T Flip- Flops modeled with Single Electron Devices	2011

M. Hasani	Half-Adder Using Silicon Quantum Dot-Based Single-Electron Transistor Operating At Room Temperature	2013
Arief Udhiarto	Two Bits Single-Electron Logic Circuit Using Double Quantum Dot Single Electron Transistor	2014
Rajanna K. M.	2–Bit Comparator Using SET Based Logic Circuits	2015

MOSES: - Monte Carlo Single-Electronics Simulator uses FORTRAN program and eventually project the transistor performance. Simultaneously the V-I characteristics is generated for piecewise time variations [48].

KOSEC(Korean Single Electron Circuit Simulation):-It is an outcome of extensive research of Korean Nano Scientist in Nano electronic laboratory, Korean University, Korea. This soft computing tool is largely dominated by Monte Carlo equation and shows high linearity with discrete property of tunneling events in SET. It has the capacity to build Coulomb blockade, Coulomb oxidation and categorically it demonstrates graphical interpretation to compare it with the SET tunneling events. The obscurity of KOSEC is that very few literature of it is made available in internet [49].

BSIM 4.O- The Berkeley Short-channel IGFET Model (BSIM) is a group-work of few intellects in the Department of Electrical Engineering and Computer Sciences (EECS) at the University of California, Berkeley. They potentially developed Mesophysics oriented precise, scalable, robust and projecting MOSFET SPICE models for circuit simulation and growth of CMOS industry. The group uses Compact Model Coalition (CMC), this is a platform for semiconductor companies and simulator vendors world-wide. It possesses the virtue of greater accuracy in modeling transistors with shorter gate length and provides efficient logarithm to quantize the non-uniformity of substrate doping. Also it provides higher frequency intended for high speed digital application. Partially it is capable to signify several diode characteristics and scholastic approach that combines the mechanism of current saturation velocity saturation and velocity overshoot as well as source-end velocity limit. Researchers additionally avail mobility and source drain resistance. Among its other merits BSIM4.0 is prolific to adopt low power consuming non-conventional MOS process. The quality assurance in compared to SPICE demonstration and has revealed greater trade-off, thereby BSIM4.0 stands to be a unique competitor in major commercial simulator formats. Besides, it provides excellent graphic user interface Agilent's IC cap that enables quick set up test bench and is intervened by real time automatic parameter extraction routine. It stands unparalleled to any bulk charging effect modelling.

BSIM 4.0 has been extensively used by Researchers to assimilate Single Electron Transistor (SET) based logic intervention into a comparatively chronological form. This aids in developing SET synthesis in a comparative sophisticated manner [50-53].

SMARTSPICE: - It offers the highest performance and accuracy required to design complex, analog and mixed signal circuits. SMART SPICE is attuned with wide spread `analog flows and foundry supplied device models'. SMART SPICE supports a wide range of models including FINFET, Bipolar and TFT. It is 100% HSPICE and SPECTRE compatible for NETLISTS, models, and offers multiple solvers and stepping algorithms. The novelty lies in the fact that it offers MC based open model development environment and extensive analog behavioral capability with Verilog-A, thereby making it capable to handle up to '400,000 active devices in 32-bit and 8 million active devices in 64-bit version' [54& 55].

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VIII. CONCLUSION

Ample study on different 'M' approaches lead to a conclusive fact that MC and ME offer high simulation time compared to MM. Although, ME and MC possess substantial accuracy and can handle Coulomb Blockade regions convincingly yet to the contrary MM suffers from low accuracy and inadequately controls Coulomb Blockade phenomenon. But this could not diminish the popularity of MM, rather it increased unilaterally as it can simulate larger SET circuit architectures compared to ME and MC based designs. Thus simulators are opted based on user specific requirements and each of the ME, MC and MM approaches are typically impetus to all substantial SET Researchers.

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