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DESIGN AND PERFORMANCE OF BAUGH-WOOLEY MULTIPLIER USING CARRY LOOK AHEAD ADDER

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ABSTRACT:

In recent year, power dissipation is one of the major challenges in VLSI design. In this project, the design and power comparison of the low power multipliers using different types of adders can be analyzed. Baugh Wooley Multiplier is one of the different methods for signed multiplication. It is not generally used. Here design and implementation of 16 bit Baugh Wooley multiplier using conventional method. This project presents an effective implementation of a high speed multiplier using the shift and adds technique of Baugh-Wooley Multiplier. This parallel multiplier usages lesser adders and lesser iterative steps. As a result of which they occupy smaller space as compared to the serial multiplier. This is very important criteria because in the fabrication of chips and high expression system requires components which are as small as possible. The comparative analysis of the design for power, delay and the area footprint has completed using Cadence RTL complier 180nm process technology. The design of carry look ahead adder for low power obtained is obtained and low power units are implemented on the future multiplier and the results are evaluated for better performance.

Keywords: Very-large-scale-integration (VLSI),Integrated Chips IC, Look Up Table(LUTs), Digital Signal Processing (DSP) ,System-on-Chip (SoC).

I.INTRODUCTION

VLSI stands for "Very Large Scale Integration". Very-large-scale-integration (VLSI) is defined as a technology that allows the construction and interconnection of hefty numbers (millions) of transistors on a single integrated circuit. Integrated circuit is a throng of one or more gates fabricated on a single silicon chip. This is the field which involves packing more and more logic devices into smaller and smaller areas. The difficulty of VLSI being designed and used today makes the manual approach to design impractical. Design automation is the edict of the day with the rapid technological developments.VLSI has been around for a long time, there is zilch new about it...but as a side effect of advances in the world of computers, there has been a dramatic rise of tools that can be used to design VLSI circuits. Alongside, obeying Moore's law, the competency of an IC has increased exponentially over the years, in terms of computation power, utilization of available area, yield.

- A stable growth in the size and hence the functionality of the ICs.
- A firm reduction in feature size and hence rise in the speed of operation as well as gate or transistor density.
- A fixed improvement in the predictability of circuit behavior.
- A sturdy increase in the variety and size of software tools for VLSI design.
- A steady escalation the integration of IC chips.

The monolithic integration of a large number of functions on a single chip usually provides,

- Less area, volume and density.
- Less power consumption.
- Less testing requirements at system level.
- High reliability, mainly due to improved on chip interconnects.

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- Higher speed of data transmission.

II.MULTIPLIERS

Multipliers play a main part in today's digital signal processing and various other applications. In great enactment systems such as microprocessor, DSP etc. Accumulation and multiplication of two binary numbers is necessary and most often used arithmetic operations. Statics shows that superfluous than 70% instructions in microprocessor and most of DSP algorithms implement addition and multiplication. So, these operation dominates the execution time.

Low power consumption is also an important dispute in multiplier design. To reduce significant power consumption it is good to reduce the number of operation thereby sinking dynamic power which is a major part of total power consumption so the need of high speed and low power multiplier has improved. Designer mainly deliberate on high speed and low power efficient circuit design. The objective of a worthy multiplier is to deliver a physically packed together, high speed and low power Consumption unit.

2.1 DIFFERENT MULTIPLIERS

A proficient multiplier should have following features

1) Accuracy: - A virtuous multiplier should give correct result.
2) Speed: - Multiplier should perform operation at high speed.
3) Area: - A multiplier should reside in less number of slices and LUTs(Look Up Table).
4) Power: - Multiplier should consume less power.

Multiplication procedure has three foremost steps:

1. Partial product generation.
2. Partial product reduction.
3. Last addition.

In place of the multiplication of an *n*-bit multiplicand per an *m* bit multiplier, *m* partial products are created and product formed is *n* + *m* bits long. Here we converse about different types of multipliers they are

1. Booth multiplier.
2. Combinational multiplier.
3. Wallace tree multiplier.
4. Array multiplier.
5. Sequential multiplier.
6. Baugh wooley multiplier.

2.1.1 Booth multiplier

Booth multiplication algorithm gives a way for multiplying binary integers in signed -2's complement illustration. Following phases are used for implementing the booth algorithm:-Let X as well as Y are two binary numbers then consuming m and n numbers of bits (m and n are the same) correspondingly.

Step 1 Making booth table: In booth table we will takings four columns one column for multiplier second for forgoing first LSB of multiplier and additional two (U and V) for partial product accumulator (P).

1. Commencing two numbers, select multiplier (X) and multiplicand (Y).
2. Proceeds 2's complement of multiplicand (Y).
3. Load X value in the table top.
4. Load 0 for X-1 value.
5. Load 0 in U and V which will take product of X & Y at the end of the operation.
6. Make n rows for separately cycle because we are multiplying m as well as n bits numbers.

Step2 Booth algorithm: Booth algorithm involves examination of the multiplier bits, then shifting of the partial product (P). Prior to the shifting, the multiplicand may be surplus to P, subtracted from the P, or left unchanged agreeing to the resulting rules:

1. Xi Xi-1
0 0 Shift only
1 1 Shift only
0 1 Add Y toward U and shift
1 0 Minus Y from U and shift

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2. Take U & V unruffled and shift arithmetic right shift which reserves the sign bit of 2's complement number. So, positive numbers also negative numbers remains positive and negative correspondingly.
3. Circularly right shift X because this will inhibit us from using two registers for the X value. Repeat the similar phases until n no. of cycles are completed. In the end we get the product of X and Y.

2.1.2 Combinational Multiplier

Combinational Multipliers look after multiplication of two unsigned binary numbers. This multiplier is also jumble-sale for the multiplication of two signed number. For each bit of the multiplier is multiplied alongside the multiplicand, the product is associated permitting to the position of the bit within the multiplier, and the ensuing products are then added to form the final result. Main gain of binary multiplication is that the peer group of intermediate products are laidback. Stipulation the multiplier bit is a 1, the product is a correctly shifted duplicate of the multiplicand; if the multiplier bit is a 0, the product is modestly 0.In maximum of the systems combinational multipliers are slow and take a lot of area.

2.1.3 Wallace Tree Multiplier

A Wallace tree multiplier is an effective hardware employment of a digital circuit that multiplies two integers invented by an Australian computer technologist Chris Wallace in 1964. Wallace tree decreases the no. of partial products and use carry select adder for the adding of partial products. In this figure blue circle symbolize full adder and red circle symbolize the half adder.
Wallace tree has three steps:-
1. Multiply apiece bit of multiplier with same bit location of multiplicand. Dependent on the position of the multiplier bits generated partial products have dissimilar weights.
2. Ease the number of partial products to two by using deposits of full and half adders.
3. After second pace we get two rows of sum and carry, add these rows by way of conventional adders.

2.1.4 Array Multiplier

Array multiplier is well known due to its regular erection. Multiplier circuit is based on repetitive addition and shifting procedure. Each partial product is spawned by the multiplication of the multiplicand by one multiplier digit. The partial product are shifted allowing to their bit sequences and then added. The summation can be achieved with normal carry propagation adder. N-1 adders are prerequisite where N is the no. of multiplier bits.

2.1.5 Sequential Multiplier

If we want to multiply two binary number (multiplicand X takes n bits and multiplier Y has m bits) with single n bit adder, we can built a sequential circuit that practices a single partial product at a time and at that point cycle the circuit m times. This type of circuit is titled sequential multiplier. Sequential multipliers are striking for their low area requirement. In a sequential multiplier, the multiplication method is separated into some sequential steps. In each step some partial products will bespawned, added to an accumulated partial sum then partial sum will be shifted to align the accumulated sum with partial product of next steps. Then, each phase of a sequential multiplication consists of three different operations which are creating partial products, adding the spawned partial products to the accumulated partial sum and shifting the partial sum.

III. PROPOSED WORK

The next peer group of wireless network requires high-throughput and low power Digital Signal Processing (DSP) ,System-on-Chip (SoC). Amongst the building slabs of a DSP system a multiplier is an essential component that has a significant role in both speed and power performance of the entire system. Now to develop the performance of DSP SoCs designing of a high-performance in addition to power efficient multiplier is crucial. The multipliers are implemented in Xilinx and matched them in terms of both Power dissipation and delay.

3.1 BAUGH WOOLEY MULTIPLIER

Baugh Wooley multiplier is considered to cater multiplication of both signed and unsigned operands, which are symbolized now the 2's complement number system. The partial products are hardened so that the negative signs are moved to the last stages, which in turn maximize the regularity of multiplication array. The Baugh Wooley multiplier is a motivating implementation of a multiplier. It produces a quite standard cell shape for easier manufacturing, while sustaining good driving features. Each full adder within the multiplier performs a similar number of computations, with the crosswise ripple carry Propagating the input signal a constant as well as similar number of times.

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3.2 ALGORITHM OF BAUGH WOOLEY MULTIPLIER

The Baugh Wooley multiplier activates on signed operands with 2's complement demonstration to make sure that the signs of all the partial products are positive. To repeat, the arithmetical values of 2's complement numbers, X and Y can be obtained using the following expressions.

The product of X and Y is expressed as

$$P = XY$$

$$= X_{n-1}Y_{n-1}2^{2n-2} + \sum_{i=0}^{n-2}\sum_{j=0}^{n-2} X_i Y_j 2^{i+j}$$

$$-X_{n-1}\sum_{j=0}^{n-2} Y_j 2^{n+j-1} - Y_{n-1}\sum_{i=0}^{n-2} X_i 2^{n+i-1}$$

It is experimental that last two positions of above equation are subtracted from partial product. To preclude the use of subtractor cells and use only adders these negative positions must be transformed. Therefore

$$-X_{n-1}\sum_{j=0}^{n-2} Y_j 2^{n+j-1} = X_{n-1}\left(-2^{2n-2} + 2^{n-1} + \sum_{j=0}^{n-2} \overline{Y}_j 2^{n+j+1}\right)$$

The product P becomes

$$P = XY$$

$$= -2^{2n-1} + (\overline{X}_{n-1} + \overline{Y}_{n-1} + X_{n-1}Y_{n-1})2^{2n-2}$$

$$+ \sum_{i=0}^{n-2}\sum_{j=0}^{n-2} X_i Y_j 2^{i+j} + (X_{n-1} + Y_{n-1})2^{n-1}$$

$$+ X_{n-1}\sum_{j=0}^{n-2} \overline{Y}_j 2^{n+j-1} + Y_{n-1}\sum_{i=0}^{n-2} \overline{X}_i 2^{n+i-1}$$

Using a gradually approach, this 2's complement multiplication algorithm can be transformed into an equivalent parallel array expression, as embraced by Baugh wooley multiplier. Wallace Tree Multiplier Baugh Wooley Multiplier are fulfilled and power dissipation and propagation delay are calculated.

To implement planned pipelined multiplier different adders specifically pseudo NMOS adder, xor & Transmission Gate, transmission gate full adder, Complementary CMOS are implemented and they are equated in rapports of power and propagation delay product pseudo NMOS has less power propagation delay product.

Architecture of baugh wooley multiplier is constructed on the carry save algorithm. It inherits the regular and iterating structure of the array multiplier.

The erection of a 4x4-bit 2's complement multiplier is shown below

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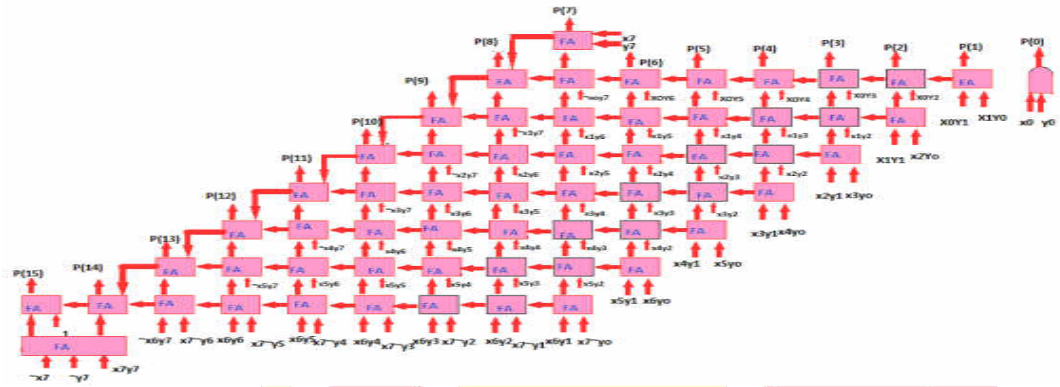

Figure1:Architecture of 8 bit Baugh Wooley Multiplier

Wallace Tree Multiplier, Baugh Wooley multiplier are realized and their power dissipations and delays of each multiplier are calculated and equated Pipelined multiplier is implemented in 180nm technology, 90nm technology and 45nm technology and their corresponding power and delay and operating frequency are calculated. Power dissipation and delay are reduced .Pipelined multiplier executed in 180nm technology has 3.1GHz operating Frequency, pipelined multiplier implemented in 90nm devises 7GHz operating frequency and 45nm technology pipelined multiplier has 9.4GHz frequency.

In this proposed work, 16*16 Baugh wooley multiplier can be designed. In the design of Baugh wooley multiplier the full adder can be replaced by the carry look ahead adder.

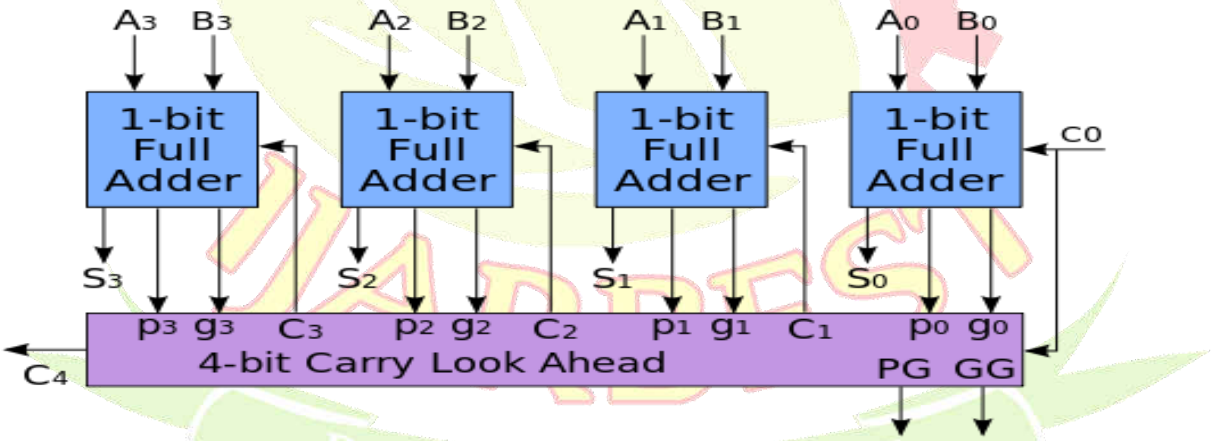

Figure:2 Carry Look ahead adder

A **carry-look ahead adder** (CLA) is a type ofadder charity in digital logic. A carry-look ahead adder improves speed by decreasing the amount of time required to determine carry bits. It can be differentiated with the simpler, but usually dawdling, ripple carry adder for which the carry bit is calculated along by the sum bit, and each bit must wait until the earlier carry has been calculated to begin calculating its own result and carry bits.The design can be implemented in Xilinx and cadence RTL at 180nm technology.In this implementation the power,delay and area consumption can be calculated.

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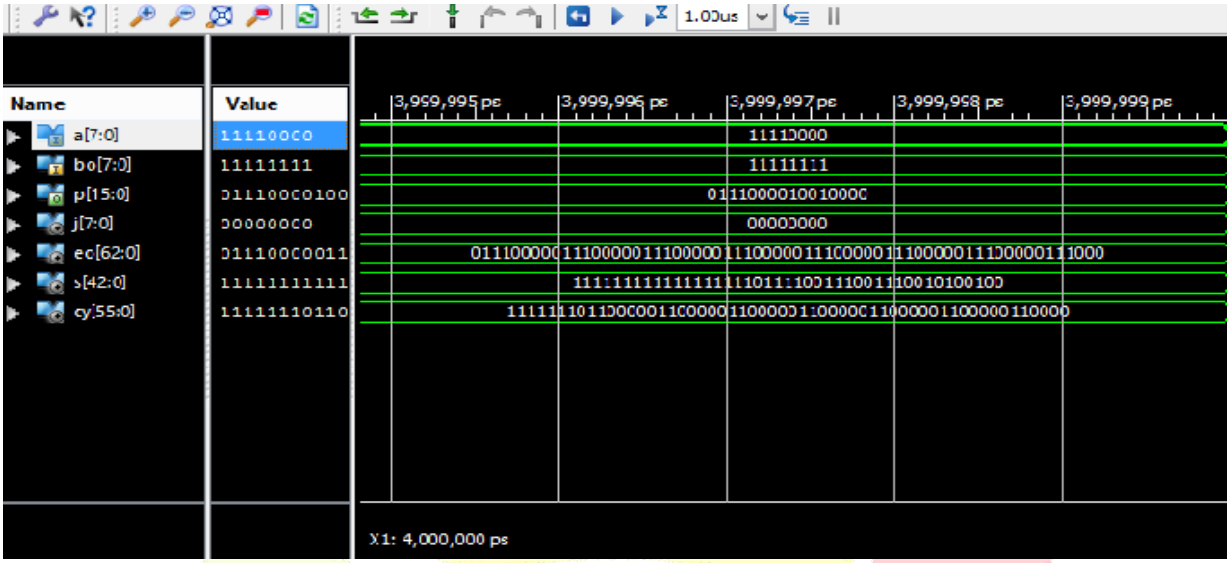

Figure:3Result for 8X8 baugh wooley multiplier

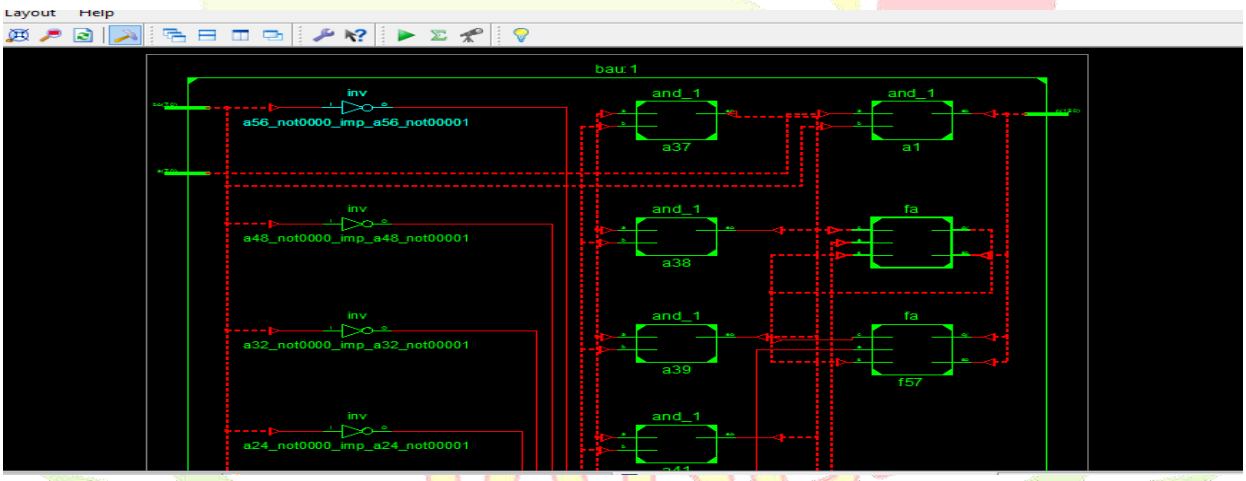

Figure:4 Schematic view of 8*8 baugh wooley multiplier

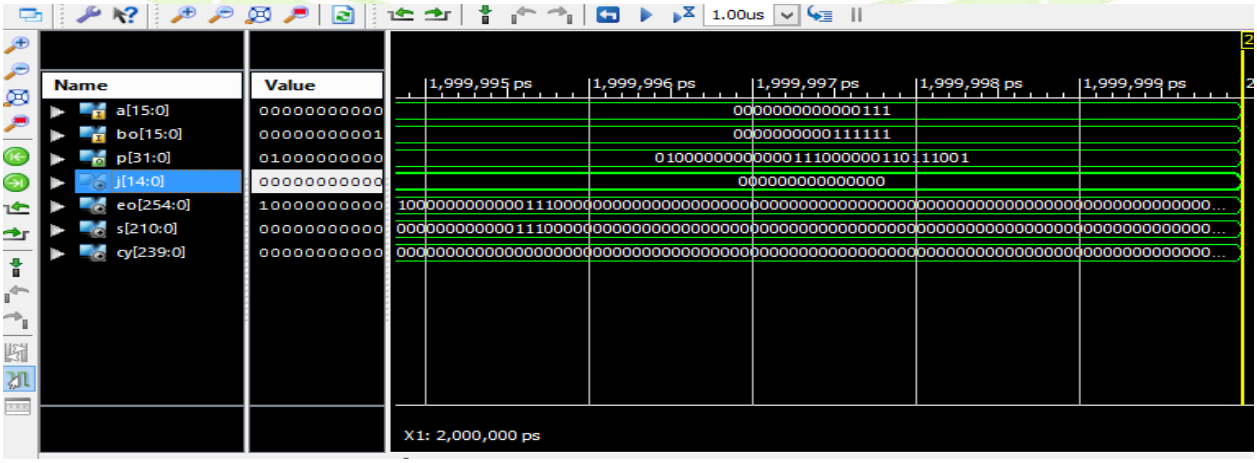

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Figure:5 Result for 16X16 baugh wooley multiplier

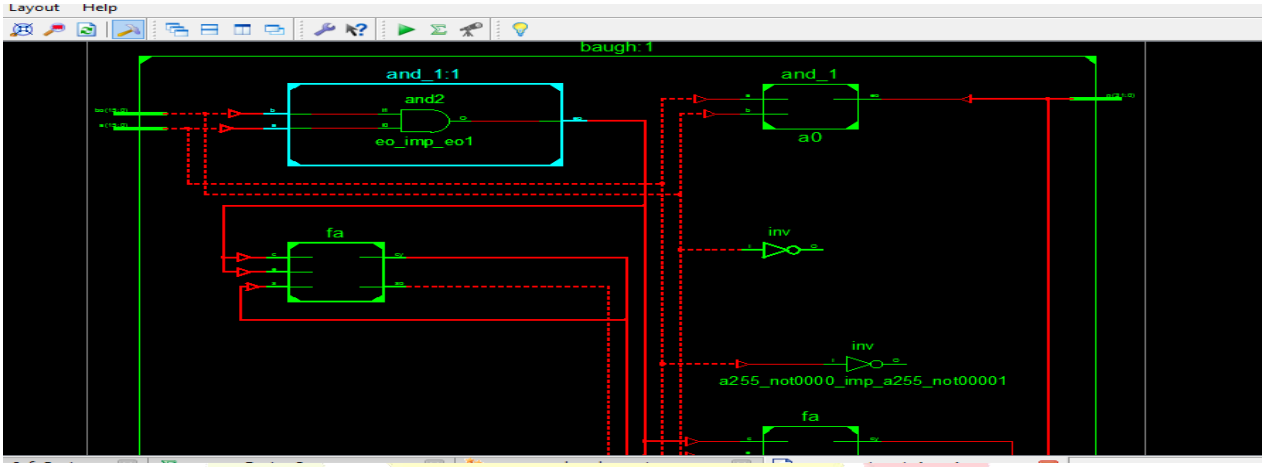

Figure:6 Schematic view16X16 baugh wooley multiplier

IV. RESULT AND CONCLUSION

In this paper the design of 8*8, 16*16 Baugh wooley multiplier can be implemented in Xilinx. The simulation result can be calculated. The schematic view of multiplier can be shown in figure. The design implementation can also implemented in Cadence with 180nm technology. The area is calculated as 10837 and power dissipation is 74.3mW and the delay is $2.37X10^{-9}$. In future, the 32*32 Baugh wooley multiplier can designed in cadence. The Carry look ahead adder can be implemented in 32*32 multiplier. The area, power and delay can be reduced by designing the Baugh wooley multiplier.

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