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FPGA BASED IMPLEMENTATION OF ECG SIGNAL ANALYSIS USING DWT

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Abstract-This paper falls within the scope of implementation of Digital Signal Processing (DSP) algorithms in the state of the art Field Programmable Gate Array (FPGA); so, it presents an FPGA-based embedded system design and its evaluation for a pre-processing stage of ECG signal analysis; such a design uses the Discrete Wavelet Transform (DWT) approach. Thus, the system deals mainly with the baseline wander (BLW) removal and the QRS detection. As the DWT-based implementation is requires important hardware resources, our system is designed, in a spirit of optimization, to fit in low-cost and low-power FPGA device for portable medical equipment. It is developed with the Xilinx design tool, System Generator for DSP which is a plug-in to Simulink. This hardware design is tested with ECG data records from the MIT-BIH Arrhythmia database. By a careful visual examination of the simulation results, we report that the whole design provides a good response especially for the part of BLW suppression; moreover, only this part concerning the BLW is tested with a JTAG Hardware co-simulation in the available board at the time of experimentation, that is the Nexys 3 board of Digilent featuring Xilinx SPARTAN 6 XC6SLX16.

Keywords- Baseline wander; DSP; DWT; ECG; FPGA; QRS detection.

I. INTRODUCTION

For over a century, electrocardiographic monitoring by means the ECG signal is one of the most widely used diagnostic tools in clinical medicine; in fact, it is applied to the patient in the prehospital setting, intensive care, emergency rooms, etc. ECG signal is the measure, via electrodes acquiring the voltage (potential difference) on the body surface, generated by the heart electrical activity. As illustrated by the figure 1, the ECG is characterized mainly by 5 waves reflecting the activity of the heart during a cardiac cycle (R-R interval); these waves are called P, Q, R, S and T; the Q, R, and S waves are treated as a single composite wave known as the QRS complex. The ECG signal is typically characterized by maximum amplitude of I mv and a bandwidth of 0.05 Hz to 100 Hz.

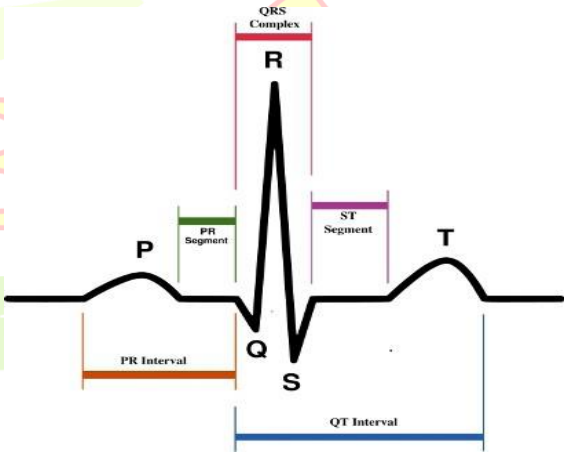

Figure 1. ECG Waveform and its Components

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Usually, the ECG analysis consists of 3 stages: preprocessing stage for providing a "clean" ECG, features extraction stage for recognition of certain ECG characteristics and decision stage for fmal diagnosis with support of medical experts. The goal of the pre-processing stage, subject of this paper, is to provide the features extraction stage with a signal free of artifacts or noises which are signals unrelated to the ECG signal.

Among these noises, the AC power line interference and the BL W produced by patient movements and respiration are by far the most dominant. Although, the QRS detection is a particular and separate operation in the ECG analysis, it can be classified as a part of the pre-processing stage, because it serves as a time reference for the features extraction stage.

In this work, we deal particularly with the baseline wander cancellation and the QRS detection using the DWT. In fact, typically the analog front-end ECG signal acquisition systems can remove in efficient manner the power line interference; however the BLW needs more digital filtering, because this artifact affects strongly the ST -segment that represents an important feature to monitor for ischemic conditions diagnosis. Our implementation is based on FPGA that has become, in the recent years, key component for implementing high performance DSP systems.

II. WAVELET TRANSFORM

For a long time, the ECG analysis is generally based on classical digital signal processing (linear filtering, Fourier Transform, etc.). But, in the past few years, many new promising approaches for the ECG analysis have emerged; among these approaches, the Wavelet Transform (WT) have been evolved rapidly and the rate of publication keeps increasing steadily [7-9]. The Fourier Transform permits the determination of the frequencies contained in a given signal; but with this tool, it can't be known when they are present for a non-stationary signal like an ECG. The WT comes then to overcome this type of problem; it transforms then the signal under investigation into another representation which presents the signal information in a more useful form, by the convolution of the signal with a function known as "wavelet". This wavelet can be moved to various locations (translation operation) on the signal and it can be stretched or squeezed (scaling operation); thus, the WT acts as a mathematical microscope at various levels of magnification.

A. Discrete Wavelet Transform (DWT)

To be calculated by computers, the WT must be discretized. As a simple sampled version of the CWT, the DWT generates redundant data, which requires an important time and more hardware resources. To overcome this problem, the widely used solution is the Mallat algorithm (pyramid algorithm) called Fast Wavelet Transform (FWT) by analogy with the Fast Fourier Transform (FFT); such an algorithm provides then sufficient information both for analysis and synthesis of the original signal, with a significant reduction in the computation time and hardware resources. It has a filter bank structure, which avoids the need to deal directly with the scaling and shifted wavelets; so, only the coefficients of the associated filter bank are required to know, permitting design, in a classic way, with Finite impulse Response (FIR) filters.

Thus, the Mallet structure algorithm with 2 levels as example; it consists of 2 stages: decomposition and reconstruction (analysis and synthesis). The signal under study x(n) is passed through several levels of set of FIR

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filters, low pass La _ D(n) and high pass Hi _D(n) , in an iterative fashion. At each level, detail component d(n) is produced by high pass filter, while approximation component a(n) is produced by the low pass filter. The reconstruction process is the reverse of the decomposition, via 2 filters, low pass La _ R(n) and high pass Hi _ R(n) . The F[R coefficients depend on the used mother wavelet, which in turn depends on the signal under investigation.

Because at each decomposition level, the frequency content is divided by 2, then each level is followed by a down sampling by 2, permitting non redundancy of data and design optimization. The process is the reverse for the reconstruction stage; thus, each level is followed by an up sampling by 2. Normally, the signal reconstruction only makes sense, after a certain treatment of the different components depending on the desired system response. Decomposition filter bank and Reconstruction filter bank.

III. SYSTEM IMPLEMENTATION

According to the Mallet algorithm, we have designed and implemented an FPGA-based embedded system for a preprocessing stage for ECG signal analysis. It deals with 2 operations, i.e. the BLW removal and QRS detection. Due to the similar structure processing for these both operations, we apply the DWT in one-step, in order to save hardware resources and execution time; this permits the implementation in a low-cost devices as proposed by [II], in this case FPGA. As rule of thumb, the mother wavelet is chooses depending on the similarity between the wavelet and the signal under investigation. In this perspective, Daubechies Wavelet shows similarities with ECG signal; so, it is used as mother wavelet. There is many orders for a given wavelet; a higher order implies a smoother wavelet and requires higher hardware resources for implementation. [n our case, we have choose the "db4" (Daubechies of order 4), which corresponds to 8-ta FIR filters, for the simulation of the whole system, based on low cost FPGA, namely the Xilinx ARTIX 7 XC7AlOOT. On another hand, due to the resources constraints of our testing board, N exys 3 board based on Xilinx SPARTAN 6 XC6SLXI6, we have used the "db2", which corresponds to 4-tap FIR filters, for the JT AG Hardware co-simulation; moreover, this experimental test, concerns only the BL W implementation. The coefficients of the different FIR filters, for both decomposition and reconstruction, are obtained by the MATLAB command "wfilters" (example for "db4"):

[Lo_D, Hi_D, Lo_R, Hi_R] = wfilters('db4')

With ECG signals from MIT-BIH database resample at a frequency of 200 Hz, the maximum frequency of ECG is then 100 Hz according to the Shannon theorem. The different bands produced by the decomposition process are as shown by the table I. The approximation all at the level 7 is chosen for the BL W removal task, whereas the detail d3(n) at the level 3 is chosen for the QRS detection task. This choice based on this analytical calculation is confirmed and consolidated by a visual inspection thanks to MATLAB tool "wave menu".

Level	Approximation	Detail
1	0 - 50 Hz	50 - 100 Hz
2	0 - 25 Hz	25 - 50 Hz
3	0 - 12. 5 Hz	12. 5 - 25 Hz
4	0 - 6.25 Hz	6.25 - 12.5 Hz
5	0 - 3.125 Hz	3.125 - 6.25 Hz

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6	0 - l.5625 Hz	l.5625 - 3.l25 Hz
7	0 - 0.78125 Hz	0.78125 - l.5625

TABLE 1: COMPONENTS FREQUENCY RANGE

The implementation is developed with the Xilinx System Generator for DSP tool, which provides system modeling and automatic optimized Hardware Description language (HDL) code generation from Simulink and MATLAB. As mentionned above, the both tasks share the some structure of the FIR filters; the figures 3 and 4 illustrate this process for low pass filters (Lo D and Lo _ R).

A. BL W removal

The BLW is a major type of noise affecting an ECG; in fact, its frequency range is usually below 0.8 Hz and, hence, overlaps with the ECG spectrum. There are a variety of approaches for BL W suppression or reduction; among these methods, the most used are the high pass filtering and cubic spline interpolation. As a promising technique, the DWT applied to the BL W removal can provide good results. The figure 5 illustrates the block diagram of our model for this task; we have adopted a solution permitting reduction in implementation resources; indeed, as can be seen, rather than we reconstruct the whole signal without a7(n) , we reconstruct only this latter and subtract it from the delayed Original ECG(n) signal; this delay depends on the time response of decomposition and reconstruction processes.

B. QRS detection

The QRS complex of the ECG signal is the reference point for almost all the ECG applications. The figure 6 shows the QRS detection structure, which is shared by many algorithms. In our case, the filtering stage ofthis detector is based on DWT and the decision stage is based on adaptive thresholding Technique and a set of heuristic rules; this detector Provides a logic signal (QRS flag), well suited for many Operations; we mention as example, but certainly not least, the heart rate calculation. The figure 8 presents the Simulink mode for this task.

IV. SYSTEM EVALUATION

Our implementation is fully simulated and partially tested via JTAG Hardware co-simulation with the Digilent Nexys 3 board based on the Xilinx Spartan-6 XC6SLX I 6 FPGA device. The System Generator for DSP tool is a plug-in to Simulink that accelerates the development of complex DSP applications on FPGA; it generates bit-true, cycle-accurate, synthesizable Veri log and VHDL code. It supports Hardware co-simulation, making it possible to incorporate a design running in an FPGA directly into a Simulink simulation. Hardware Co-Simulation compilation creates a bit stream and associate it to a block. When the design is simulated in Simulink, results for the compiled portion are calculated in hardware. This allows the compiled portion to be tested in actual hardware and can speed up simulation dramatically.

ECG signal used for the different tests are obtained from the MIT-BIH Arrhythmia database [19]. By a careful visual examination of the simulation results, we report that the whole design shows a good response especially for the part of BL W suppression; moreover, only this part concerning the BL W is tested with a Hardware co simulation in the available board at the time of experimentation, that is the Nexys 3 board of Digilent featuring Xilinx's SPARTAN 6 XC6SLXI6. The figure 10 shows a small episode of the response for the record "108", which is among the records severely distorted by

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BLW in the MIT-BIH database. We note particularly the good detection of the BLW; the signal BLW(n) follows exactly the wandering of the noised original signal, ECG(n) with (BLW). As a global evaluation, mainly based on a careful visual Inspection, we can report that this implementation is successful particularly for the BLW. We find that the QRS detection yields good results, but with lower performance compared to implementation with linear filtering as reported in; indeed, in the context of this comparison, we estimate its accuracy around 94% with largely more required hardware resources.

In terms of the FPGA resources utilization, the table II

presents the results for:

• The simulation on low-cost low-power FPGA, i.e. the Xilinx ARTIX 7 XC7AlOOT.

• The JT AG Hardware co-simulation on the available board at the time of experimentation, i.e. the Nexys 3 board featuring Xilinx SPARTAN 6 XC6SLXI6;

CONCLUSION

In this work, we have investigated the ability of the wavelet analysis to process the biomedical ECG signal, particularly the QRS detection and the BL W cancellation. The implementation is based on a small and low-cost FPGA, i.e. the Xilinx ARTIX 7 XC7AIOOT, using the DWT according to the Mallat algorithm. The system is developed in the system generator for DSP tool, plug-in to Simulink. The system simulation was successful and due the resources constraints, only a part of system, i.e. the BLW suppression, was tested with JTAG Hardware co-simulation in the Nexys 3 board from Digilent; it was particularly successful.We report that, although the 5Implementation of DSP systems based on DWT produces good results, it requires more resources compared to the Implementation based on classic linear filtering. So, more investigation must be done to optimize such 5Implementations, in terms of resources utilization and response time. We think that such optimized Implementations can be used as)P cores connected to bus in soft processor-based systems; in the case of Xilinx, the soft processor is the MicrobBiaze and the bus can be PLB or AX) or FSL. In this way, these IP cores act as soft co-processors.

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