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NEW HIGH PERFORMANCE 4 BIT PARALLEL ADDER USING DOMINO LOGIC

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Abstract

The aim of the project is to design a low power performance using four bit parallel adder. The main objective is to minimize the power consumption and to reduce the area from the existing technique a low power full adder using domino approach is analyzed and it shows a comparative analysis of proposed full adder with other full adders using static approach. The result shows that the proposed 22T domino full adder consumed 14% less power as compared to 10T static full adder 6% less power consumed as compared to 28T static full adder and 8% less power consumed as compared to 27T domino full adder. The proposed system is a new high performance of 4-bit parallel adder using domino approach. Here full adder using 22T is connected in series and the output is taken by the MICROWIND tool 3.0. The main application of this concept is specific DSP architectures and microprocessors.

Keywords:
AREA, POWER, STATIC, DYNAMIC, DOM

1. INTRODUCTION

To increase the performance of VLSI circuits and integrate more functionality into every chip, the size of the transistor is continually shrinking day by day which results in the complexity of chips and circuit power consumption. Now a day, designing

of low power and VLSI circuits is one of the biggest challenges. Also power and delay parameters of any VLSI circuit can't be reduced at the same time, but we can optimize these two parameters.

There are three major contributions to power consumption in CMOS circuits. One is the active power due to discharging and charging of the circuit capacitances during switching and the other is leakage power due to leakage current and the third is short circuit currents that flow directly from the supply to ground when the n-sub network and the p-sub network of a CMOS gate both conduct simultaneously. As we scale down the supply voltage for reducing the power that decreases the threshold voltage (Vt) and gate oxide thickness (tox) of the transistor, which leads to increase in sub-threshold leakage (I sub) current. So many techniques have been proposed to decrease the transistor count and consequently decrease power consumption and area like low swing techniques and the multiple supply technique and the dual Vt

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technique, but these techniques are helpful to reduce the power consumption, but at the same time they may degrade the speed and weaken the noise immunity of the circuits.

1.1 Dynamic Logic

Dynamic logic requires a minimum clock rate fast enough that the output state of each dynamic gate is used or refreshed before the charge in the output capacitance leaks out enough to cause the digital state of the output to change, during the part of the clock cycle that the output is not being actively driven. Dynamic logic when properly designed can be over twice as fast as static logic. It uses only the faster n-transistors, which improve the transistor sizing optimizations. In general, dynamic logic greatly increases the number of transistors that are switching at any given time, which increase power consumption over static CMOS. There is several power saving techniques that can be implemented in a dynamic logic based system. Dynamic logic is temporary (transient) in that output levels will remain valid only for a certain period of time it is normally done with charging and selectively discharging capacitance (i.e. capacitive circuit nodes)

- Precharge clock to charge the capacitance
- Evaluate clock to discharge the capacitance depending on condition of logic inputs

i)Dynamic Bootstrapping Technique

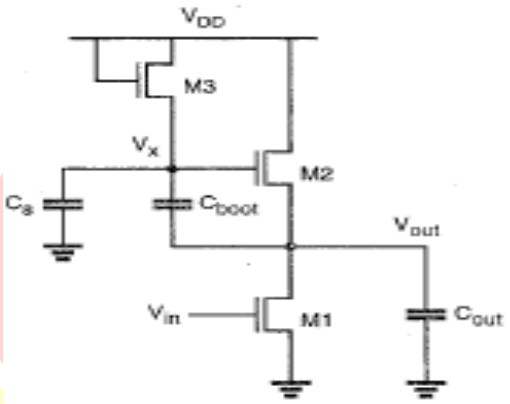

Fig.1.1 Dynamic circuit diagram of bootstrapping technique

Bootstrapping is a technique that is sometimes used to charge up a transistor gate to a voltage higher than Vdd when that transistor has to drive a line to the full Vdd. At left is a NMOS bootstrap driver often used in memory circuits to drive a highly capacitive word line.

1.2 Static Logic

In static CMOS logic the output is connected to ground through an n-block and to VDD through a dual p-block. Without changes of the inputs this gates consumes only the leakage currents of some transistors

1.3 Domino Logic

Domino logic is a CMOS based evolution of the dynamic logic techniques based on either PMOS or NMOS transistors. It allows a rail-to-rail logic swing. It was developed to speed up circuits. Actually coming up with a domino chain to do that is pretty complicated.

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1.4 Bit Parallel Adder

The 4-bit parallel adder is constructed by cascading full adders (FA) blocks in series. One full adder is responsible for the addition of two binary digits at any stage of the ripple carry. The carryout of one stage is fed directly to the carry-in of the next stage. A number of full adders may be added to the ripple carry adder or ripple carry adders of different sizes may be cascaded in order to accommodate binary vector strings of larger sizes. For an n-bit parallel adder, it requires n computational elements.

One of the most serious drawbacks of this adder is that the delay increases linearly with the bit length. As mentioned before, each full adder has to wait for the carry out of the previous stage to output steady-state result.

2. Low Power Full Adder Design

There are several different techniques to reduce power consumption in CMOS full adder circuits

• For reducing the dynamic power output and input capacitance values can be minimized.

• For reducing the short and static power, avoid using both Vdd and GND simultaneously in circuit's components.

3. Full Adder

A.28T Basic Static Full adder

28T static based, full adder is the basic structure for any arithmetical circuit as shown in fig.1. A, B, C are the inputs and Sum and C_{out} are the outputs of full adder [6].

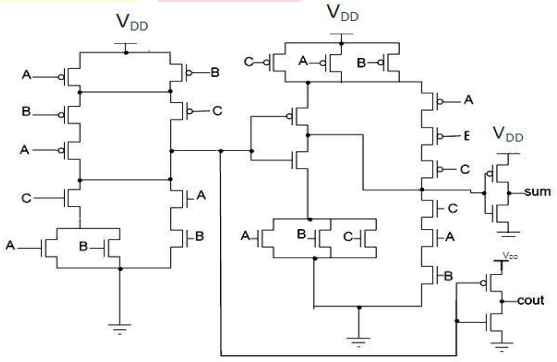

Fig.3.2 full adder using 28 Transistors

The basic structure for any arithmetical circuit requires 28transistors counts that designed by static logic approaches as shown in Fig.3.2. Static based, full adder is the basic structure for any arithmetical circuit.

B. 10T Static Full Adder

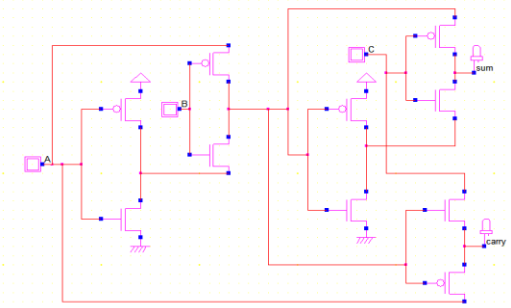

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Fig.2 full adder using 10 Transistors

The full adder circuit using static logic approach and implemented using only 10 transistors. The four-transistor XNOR module also used in it.

C. 27T Domino Full Adder

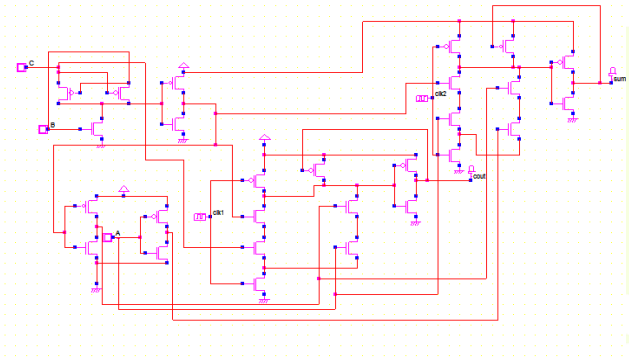

Fig.3 Circuit diagram of domino full adder using 27transistors

The third full adder based on domino logic style, uses27 transistors. It is based on 3-transistor implementations of the XOR and XNOR functions presented in, pass transistors, and transmission gates as shown in Fig.3.3 . Dynamic logic is one which gives the output with clock as an initiative for a combinational circuit.

D. 22T Domino Full Adder

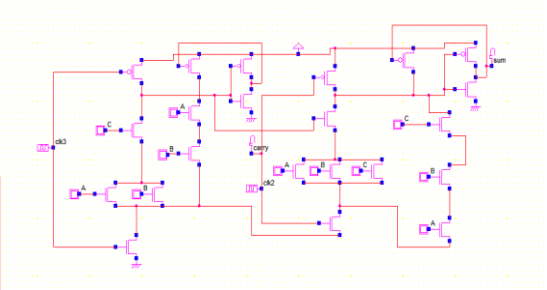

Fig.4 Circuit diagram of domino full adder using 22 transistors

In this circuit as shown in Fig.3.4.there is no direct path between V_{dd} and GND and discharge of transistor depend on the clock. In the proposed design, during pre-charging phase clock is low and dynamic node is charged. During evaluation phase clock becomes high

4.EQUATIONS

Full adder implementation is designed in a dual-rail configuration, which is elaborated on in the design strategy section. The full adder has a third input in addition to A and B: the carry in signal C_{in}.

$S=A \oplus B \oplus C_{in}$……(1)

$C=AB+BC_{in}+C_{in}A$……(2)

Where S is the sum, C is the input carry, and A and B are the inputs.

5.SIMULATION RESULTS

10T STATIC FULL ADDER

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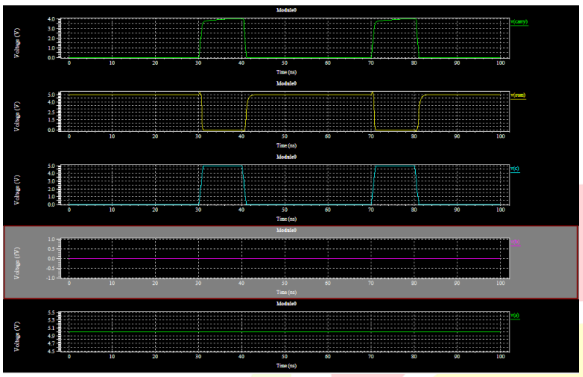
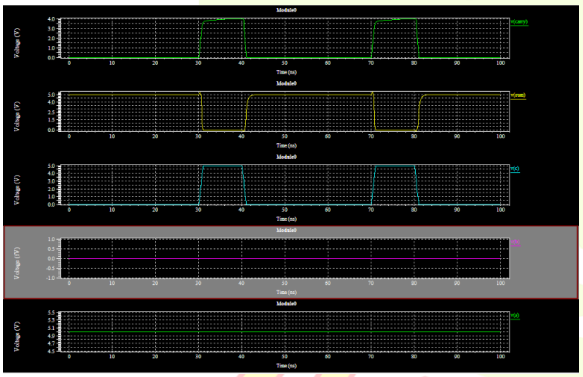


22T DOMINO FULL ADDER



6.PROPOSED METHOD

By comparing many logics with domino the pass transistor logic(PTL) is better. It reduces the count of transistors used to make different logic gates by eliminating redundant transistors.

I. PASS TRANSISTOR LOGIC

It act as a switch which pass the logic levels between nodes of a circuit, instead of using switch connected directly to a supply voltage. It reduce the transistor count.

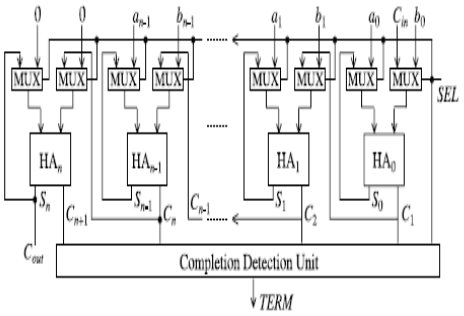


Fig 6.1 4bit parallel adder using PTL

1. 4-bit parallel adder using pass transistor logic

In pass transistor logic the input is given to both source and drain also.

In pass transistor logic only n-MOS is preferred than p-MOS. Because,n-MOS full of electrons.So, n-MOS travel faster than p-MOS.

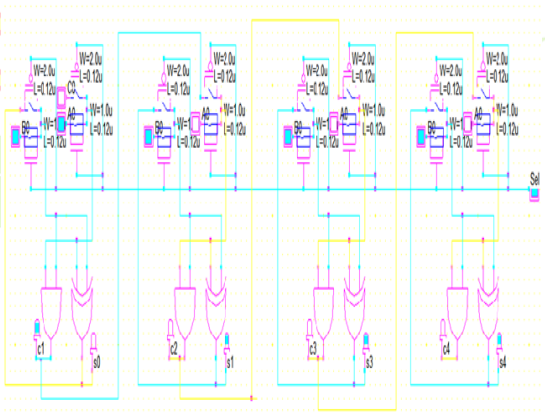


Fig6.2 4bit parallel adder using PTL

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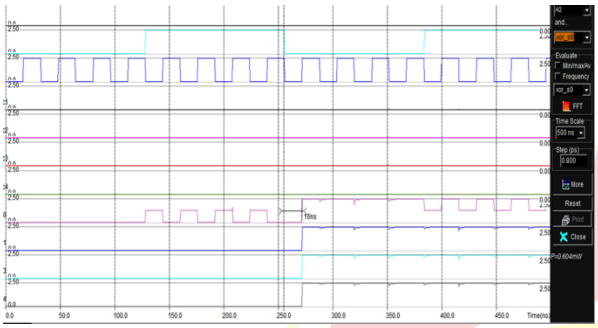

Fig6.3 Ouput waveformof 4bit parallel adder using PTL

7. COMPARISION TABLE

Table 7.1 Comparison of different logics using Full adders

TRANSISTORS	POWER (mw)	AREA (µm)
22T Domino Full Adder	1.23	115.5O
4 Bit Parallel Adder Using Domino Logic	4.101	321.00
Full Adder Using PTL	0.737	23.37
4 Bit Parallel Adder Using PTL	0.604	35.00

9.CONCLUSION

It has been concluded that 4-bit parallel adder using 22T domino logic shows minimum power consumption, and area as compared to the other full adder circuits. As domino logic based circuit consumes more power as compared to static logic but still optimizing a power in proposed circuit, 22T domino full adder show 1.4 times less power consumption as compared to 28T static full adder circuit and 0.14 times less power as compared to 10T static full adder. So 4- bit parallel adder using 22T domino circuit shows the best result among the 28T, 10T, 22T full adder and also shows minimum power and area. The simulation is carried out by the MICROWIND 3.0.

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