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A Novel Design of Active Neutral Point Clamped Flying Capacitor Five Level Inverter Using Multicarrier PWM.

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Abstract:

This paper proposes a brand new 5-degree hybrid topology combining features of impartial point clamped and flying capacitor inverters. The proposed topology offers a change off between exceptional thing counts to obtain an awesome loss distribution, keep away from direct series connection of semiconductor gadgets, hold the balanced operation of dc-link capacitors even as keeping the number of pricey additives such as capacitors and switches low.

Keywords— Multilevel Inverter, Flying Capacitor, Active Neutral Point Clamped, Diode Clamped

Introduction:

Because of the growing demand on the renewable strength assets, grid connected inverter structures are getting an increasing number of critical than ever earlier than [1,2]. For grid -linked operation, the inverter must meet the subsequent necessities.

1. The inverter has to generate a pure sinusoidal output voltage.

2. The inverter output current have to have low general harmonic distortion (THD).

Traditionally, two-stage PWM inverter is used for grid-tied operation. In case of a -stage inverter, the switching frequency need to be excessive or the inductance of the output filter inductor need to be large enough to fulfill the desired THD. To cope with the issues associated with the two-degree inverter, multi-level inverters (MLIs) are brought for grid connected inverter. numerous MLI topologies had been advised to date and they may be especially categorized as 3 kinds in Fig. 1; neutral factor clamped (NPC), flying capacitor(FC), and cascaded type .gain of the MLIs is that their switching frequency and device voltage rating may be lots decrease than the ones of at extra two-degree inverter for the same output voltage. Consequently, IGBT switching loss can be decreased substantially and therefore the inverter gadget efficiency may be expanded .in this paper, a circuit primarily based on a H-bridge topology with 4 switches linked to the dc-link is proposed as a MLI topology. Fig. 2 indicates the proposed MLI. Additionally it is simple because the proposed PWM method makes use of one provider sign for producing PWM signals. Similarly, the switching collection considering the voltage stability of dc-link changed into proposed. Subsequently, the proposed topology of the multi-level inverter is verified by means of showing the feasibility via the simulation and the test.

Existing system:

NPC inverter makes use of diodes to clamp the voltage ranges generated on the dc-hyperlink capacitors to the output. Excessive number of diodes, unbalanced operation of dc-link's voltage divider capacitors, and choppy distribution of loss among switches are foremost issues of this topology. The disadvantages of FC-ANPC are high number of

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switches, collection connection of high voltage switches, and negative loss distribution.

Proposed system:

This paper proposes a brand new five-stage hybrid topology primarily based on FC and NPC inverters. The goal of the proposed topology is to overcome the shortcomings of the conventional FC-ANPC. Therefore, comparatively, the proposed topology offers better loss distribution, avoids direct series connection of high voltage switches, and eliminates 2 switches in step with section leg. these benefits come on the price of an extra capacitor and 6 diodes. Though, the lifetime of each capacitor is anticipated to extend due to the half of cycle operation and decrease rms cutting-edge. number of devices of the proposed multi-stage inverter is decrease than that of the traditional multi-degree inverters. Consequently, the proposed device is extra dependable and cost aggressive than the traditional two-degree and multilevel inverters. in the H-bridge converter are operated at a low frequency (e.g. 60 Hz) frequency. Therefore, switching loss of the four switches nearly negligible. handiest one carrier signal is required to generate the PWM signals .The proposed topology may be without difficulty prolonged to 5-stage or higher level with minimized lively device factor remember.

Operation of proposed topology:

The proposed topology consists of a dc-hyperlink this is not unusual most of the 3 phases. The dc-hyperlink offers three voltage degrees +2E, zero, and -2E for the section legs. since all the stages have similar configuration, most effective one phase leg of the proposed topology has been shown in Fig. 1. all the additives shown in the discern have equal working voltage E i.e. one fourth of the dc-link voltage Vdc. The flying capacitors CA1 and CA2 are controlled to stay charged at the goal voltage E. The to be had states of one segment leg are shown in desk I. To generate level 2E, all of the pinnacle arm switches SA1, SA2, SA3, SA4 must switch on. For stage E, choices are to be had i.e. either via dc-link's fine point (EP) or through dc-link's neutral factor (E0). This redundancy can be used to stability the voltage of CA1. Degree 0 is generated thru clamping the dclink's neutral point to the output (00). bad states may be generated similarly because of the symmetry of the topology. The operation of this topology is in essence much like topologies which include stacked multicell (SMC) converter , wherein the positive and negative stacks operate independently. Subsequently, the nice stack capacitor CA1 is used and balanced during the fantastic cycle and rest for the duration of the terrible cycle, while the terrible stack capacitor CA2 is used and balanced at some point of the terrible cycle and relaxation throughout the superb cycle. So, the flying capacitors will see the switching frequency in preference to line frequency and therefore the capacitor size is not too huge. much like the 3-degree NPC inverter, if the 3 phases of the load are balanced, the neutral point voltage will be regular in principle. however, the voltage might barely waft away due to the imbalance in the elements' leakage present day. In addition, despite the fact that small, there's continually a few imbalance among the stages. A steady voltage go with the flow, even though small, can cause higher voltage throughout a part of the devices that may be lethal. Nonetheless, this waft can be compensated via injecting a small common mode to the 3 phases. An important feature of the proposed topology is the even distribution of transitions amongst switching gadgets. Therefore, switching loss which is the predominant limiting element of inverter's thermal performance is shipped a number of the switches. Because the fundamental result, the tradeoff between switching frequency and modern dreading is progressed. This gives the opportunity to both increases the rated modern and energy of the inverter or growth the switching frequency resulting in decrease capacitor size and improved voltage waveform exceptional.

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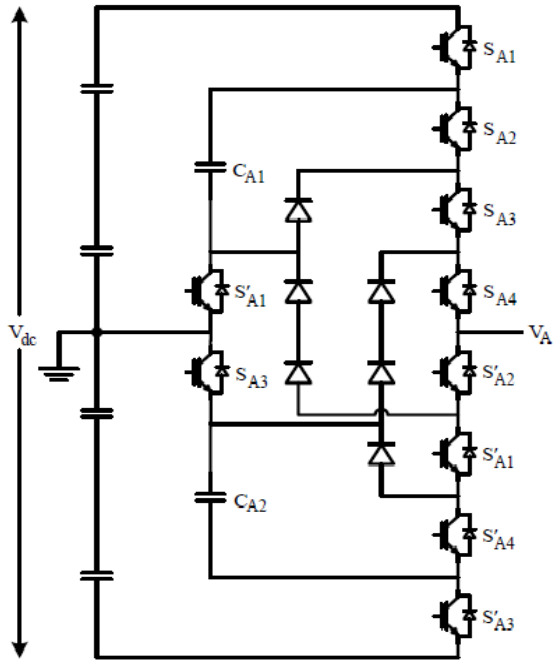

Fig. 1. A phase leg of the proposed 5-level hybrid topology.

Carrier based modulation:

Provider set's association and reference waveform's shape are the main resources of sorts in service-based totally modulation techniques for multilevel inverters. As for provider set's arrangement, stage shifted companies LSC and section shifted vendors p.c are the two predominant categories which might be respectively suitable for diode-clamped and multi-mobile structures. two members within the LSC own family, opportunity segment opposition disposition APOD and section disposition PD are known to generate the satisfactory outcomes for singe-segment and three phase programs, respectively. % in its authentic form has been shown to generate a PWM waveform that matches with APOD. also a modified model of percent with dynamic phase shift has been proven to suit with PD . The reference for unmarried-section programs is mostly a easy sinusoidal waveform. For 3-section packages, a variety of reference waveforms are to be had due to the opportunity of commonplace mode injection in 3-section structure. this adaptability has been used to serve one-of-a-kind functions such as improved dc hyperlink usage, decrease THD, lower Loss, and impartial factor voltage manipulate. For the proposed inverter, a hybrid modulation approach is required because of the hybrid shape of the topology. parent 3 illustrates the modulation technique for single-phase case. it's far intuitive to separate the operation to effective and negative cycles, seeing that every cycle is generated with a 3-degree FC stack. The gate signals for every FC is then generated the use of % to provide herbal voltage balancing for the flying capacitors. The generated output PWM waveform fits the APOD scheme.

Non-carrier modulation:

For non-carrier-primarily based modulation strategies which include SVM and she or he, the output PWM waveform can be generated first and then decomposed to the specified switching signals. Determine 4 illustrates the required manner to generate the gate signals for each section leg. The 5-level PWM waveform is first separated to advantageous and bad cycle 3-stage PWMs. Using nation system decoder, each cycle is then decomposed to two 2-level PWMs i.e. the specified gate indicators for each FC mobile. it's far important to word that this procedure is impartial of the followed modulation method. Consequently, it may be used with carrier-primarily based modulation strategies in addition to non carrier- primarily based. This might be a great alternative when the complexity of the service-based method is enormously excessive e.g. for PD scheme.

It is important to note that this procedure is independent of the adopted modulation technique. Therefore, it can be used with carrier-based modulation techniques as well as non-carrier-based. This might be a good alternative when the complexity of the carrier-based technique is relatively high e.g. for PD scheme.

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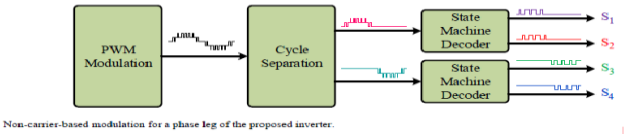
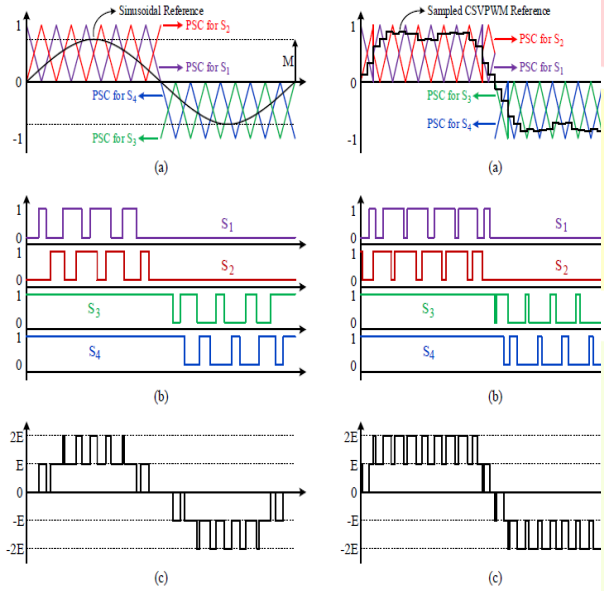


Non-carrier-based modulation for a phase leg of the proposed inverter.

Fig. 2. Carrier-based modulation using PSC with sinusoidal reference for single phase application. (a) Reference and carriers arrangement. (b) Gate signals. (c) Output waveform.

Fig. 3. Carrier-based modulation using modified PSC with samp CSVPWM reference for three phase application. (a) Reference and carri arrangement. (b) Gate signals. (c) Output waveform.

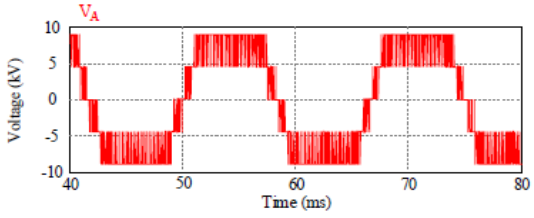


Comparison with Other Topologies:

A evaluation among the proposed topology and unique 5-degree topologies in phrases of factor count number and loss distribution is listed in table II. The 5-stage NPC has low switch count however the predominant issues are unbalanced operation of dc-hyperlink capacitors, terrible loss distribution among switches, and immoderate range of diodes. 5-degree FC gives low transfer matter and fantastic loss distribution but calls for high variety of flying capacitors which could adversely affect the initial fee, preservation and substitute surcharges, and reliability of the inverter. Capacitors' Precharge requirement in some programs is likewise a drawback of this topology. The five-level SMC topology provides decrease capacitor rely as compared to FC and top loss distribution. But, excessive transfer count and excessive frequency switches in series are the principle issues of this topology. The five-stage FC ANPC presents an amazing balance among the quantity of semiconductors and capacitors. The main trouble with this topology is the negative loss distribution many of the switches. The topology proposed in this paper, affords a tradeoff between distinct factor counts to gain a great loss distribution, avoid direct series connection of semiconductor gadgets, hold the balanced operation of dc link capacitors whilst preserving the variety of highly-priced components together with capacitors and switches as small as viable.

Simulation Results:

To verify the operation of the proposed topology and the performance of the modulation techniques provided in section III, a model is developed and simulated with PSIM software. The performance of the natural balancing technique for a three-phase 12kV inverter supplying a 5MVA load at power factor of 0.7 is shown in Fig. 5. Centered space vector modulation (CSVPWM) is used at modulation index of 1.09 and carrier



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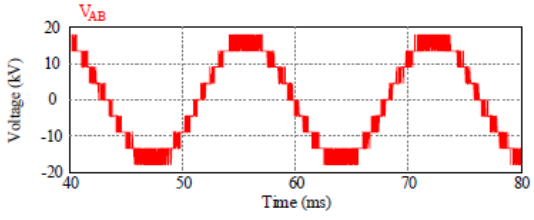

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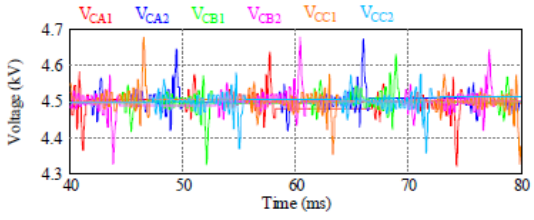

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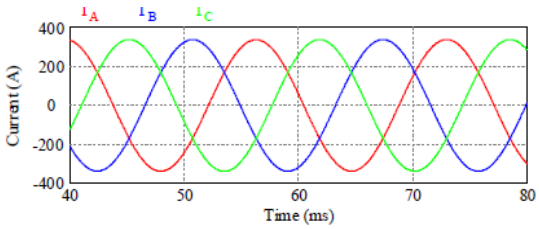
Fig. 5. Simulation results. (a) Phase voltage (b) Line voltage (c) Flying capacitor voltages (d) Load current



COMPARISON OF DIFFERENT TOPOLOGIES

Topology	Flying Capacitors	Switches	Diodes	Loss Distribution
5L-NPC	0	8	12	Poor
5L-FC	6	8	0	Excellent
5L-SMC	2	12	0	Good
5L-FC-ANPC	1	12	0	Fair
Proposed Topology	2	10	6	Good

Conclusion:

A new hybrid 5-stage inverter topology and modulation approach is proposed. in comparison to five-degree ANPC because the maximum similar topology, this new topology requires much less switches on the price of an additional capacitor and 6 diodes. However, for the reason that capacitors nonetheless see the switching frequency and their size remain the same, it's miles anticipated to lessen the inverter's general cost. Additionally, in contrast to five-stage ANPC, all switches need to face up to the equal voltage which removes the need for collection connection of switches and associated simultaneous turn on and rancid trouble. Accurate loss distribution among switches cans growth the inverters rated electricity or offer higher switching frequency and smaller capacitor size.

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