ISSN 2395-695X (Print)
ISSN 2395-695X (Online)

International Journal of Advanced Research in Biology Engineering Science and Technology (IJARBEST)
Vol. 2, Special Issue 14, May 2016

An Area Efficient FFT Implementation for OFDM

R.KALAIVANI[#1], Dr. DEEPA JOSE[#1], Dr. P. NIRMAL KUMAR[#3]

[#]*Department of Electronics and Communication Engineering, Anna University Guindy, Chennai, India*

[1]kalai512mit@gmail.com

[2]deepa.ece@kcgcollege.com

[3]nirmal2100@yahoo.co.in

***Abstract*— Multiplier less Inverse Fast Fourier Transform is a efficient technique for designing an orthogonal frequency division multiplexing based digital transmitter. OFDM plays a vital role in wireless systems like IEEE 802.11x and IEEE 802.16x. In this paper, an efficient way of FFT implementation has to be done. This works mainly concentrates on reduction of hardware complexity and power consumption due to the complex multiplication involved in twiddle factors at the input stage of IFFT processing unit. This trivial multiplication can be replaced by concepts of 'pass-logic' which eliminates the multiplication factor in butterfly module. This technique optimises the FFT structure with less power and less area. The comparison of various N point FFT with multipliers and pass-logic has been tabulated. The performance improvement of FFT has to be analysed. The proposed architecture with pass logic is an encouraging phenomenon in OFDM based wireless systems.**

Key words: FFT, Inverse Fast Fourier Transform, OFDM, pass-logic, twiddle multiplier

I. INTRODUCTION

Fast Fourier Transform plays a vital role in a modern digital signal processing and telecommunications, especially in orthogonal frequency division multiplexing systems, such as wired and wireless systems. Orthogonal frequency division multiplexing (OFDM) will suitable for video transmission and mobile Internet applications. OFDM techniques have received great attention in high-speed data communication systems and have been selected for wireless local area network IEEE 802.11a and Hiperlan-2, digital audio broadcasting, digital video broadcasting, very high-speed digital subscriber line, and beyond 3G research. In general, FFT and IFFT are used as a digital transmitter and receiver in the OFDM systems.

The computational complexity in FFT processor unit increasing as the number of sample point increases. Therefore, the practical implementation of FFT limits the power consumption, silicon area and bit processing rate. The efficiency of FFT unit is improved by redesigning the arithmetic units, modifying the structure and adopting the modulation aware multipliers, choosing the pipeline strategy and redesigning the memory controller.

A novel pass-logic technique is introduced to reduce area, power and to improve the performance. The proposed method simplifies the hardware complexity at the input stage of N-point inverse FFT structure. This paper describes about the implementation of IFFT technique with pass logic and multipliers and comparison of various parameters have been analyzed. The results produced have been compared with normal FFT multiplier techniques. This comparison shows pass logic technique is the better one in terms of power, area and delay. However, the basic FFT structure cannot provide the better performance due to computationally intensive tasks.

A. RADIX-2 DIF FFT ALGORITHM

The most basic FFT algorithm is the Radix-2 Decimation in frequency algorithm. This algorithm decomposes even and odd-indexed frequency samples shown mathematically in equation set as

$$x(2k) = \sum_{n=0}^{N-1}[x(n)W_N^{2kn}]$$

$$= \sum_{n=0}^{\frac{N}{2}-1}[x(n)W_N^{2kn}] + \sum_{n=0}^{\frac{N}{2}-1}[x(n+\tfrac{N}{2})W_N^{2k(n+\frac{N}{2})}]$$

$$= \sum_{n=0}^{\frac{N}{2}-1}[x(n)W_N^{2kn}] + \sum_{n=0}^{\frac{N}{2}-1}[x(n+\tfrac{N}{2})W_N^{2kn}$$

$$= \sum_{n=0}^{\frac{N}{2}-1}[(x(n)+x(n+\tfrac{N}{2}))W_{\frac{N}{2}}^{kn}]$$

$$= DFT_{\frac{N}{2}}\left[x(n)+x(n+\frac{N}{2})\right]$$

$$x(2k+1) = \sum_{n=0}^{N-1}[x(n)W_N^{(2k+1)n}]$$

$$= \sum_{n=0}^{\frac{N}{2}-1}[(x(n)+W_N^{\frac{N}{2}}x(n+\tfrac{N}{2}))W_N^{(k+1)n}]$$

ISSN 2395-695X (Print)
ISSN 2395-695X (Online)
International Journal of Advanced Research in Biology Engineering Science and Technology (IJARBEST)
Vol. 2, Special Issue 14, May 2016

$$= \sum_{n=0}^{\frac{N}{2}-1} \left[\left(x(n) - x\left(n + \frac{N}{2}\right) \right) W_N^n W_{\frac{N}{2}}^{kn} \right]$$

$$= DFT_{\frac{N}{2}} \left[\left(x(n) - x\left(n + \frac{N}{2}\right) \right) W_N^n \right]$$

The decimation in frequency FFT algorithm decomposes the DFT by recursively splitting the sequence elements X (k) in the frequency domain into smaller and smaller sub sequences. The algorithm carries complex addition and complex multiplication operation. These computations are done in radix 2 butterfly structure as shown in figure. This is similar to DIT algorithm except the inputs are given in normal order and outputs are taken in bit reversal order and twiddle multipliers are multiplied after the addition operation.

B. Design of DIF FFT architecture with pass logic

In OFDM system N-point radix-2 Inverse FFT is implemented on transmitter side which has n stages. This architecture has maximum number of twiddle multipliers at the input stage (nth stage). The inputs at the nth stage are converted into 'w' bits which follows any one of the value {0, TF,-TF}, where TF represents twiddle factor. The proposed pass-logic passes inputs as {0, 1, -1} and TF, which can replaces the twiddle multiplication at the nth stage of each butterfly structure. In R2-DIF-FFT architecture represented in Fig.1used in the OFDM based transceiver shows the number of frequency divisions with respect to complexity in N point FFT. The complexity of N point FFT can be presented in the Table I describes the number of stages, (N/2 $\log_2$ N) total multipliers and there are 2^n-1 number of multipliers used in nth stage of FFT unit. The hardware complexity would certainly reduced by the proposed pass logic.

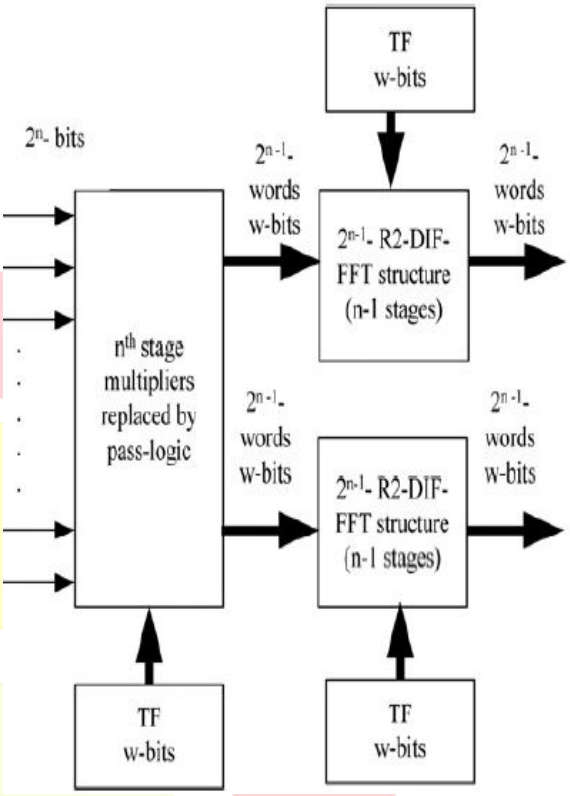


Fig.1 R2 DIF-FFT architecture

TABLE I
COMPLEXITY IN N-POINT FFT UNIT

FFT Stages (n)	FFT points (N=2^n)	Total multipliers (N/2log2N)	Multipliers used in nth stage (2^n-1)
3	8	12	4
4	16	32	8
5	32	80	16
6	64	192	32
7	128	448	64
8	256	1024	128
9	512	2304	256

II. Pass- logic

The proposed PL is illustrated in Fig.2 eliminates the number of multipliers available at the nth stage of DIF FFT architecture. This module accepts the input as {0, +1,-1} which can be replaced by two bit data {00, 01 and 11} and a TF where a and b are the real and imaginary inputs which has (w+1) bits in signed magnitude form. The truth table for PL is shown in table II for various input combinations output is obtained.

ISSN 2395-695X (Print)
ISSN 2395-695X (Online)
International Journal of Advanced Research in Biology Engineering Science and Technology (IJARBEST)
Vol. 2, Special Issue 14, May 2016

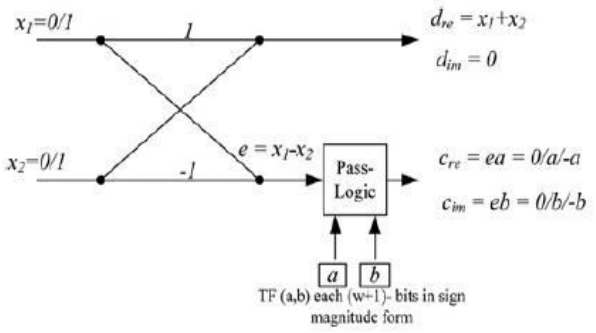


Fig 2 R2 butterfly with PL (used only in input/nth stage)

Fig.3 illustrates the pass logic module, all the redundant adders and bit-shifters are eliminated by using PL technique. In general 'w-bit' multiplier algorithm will require (w − 1) numbers of (2w − 1) bit adders and (w − 1) number of shift operations to meet the worst data cases. Hence the power required and hardware complexity are considerably reduced.

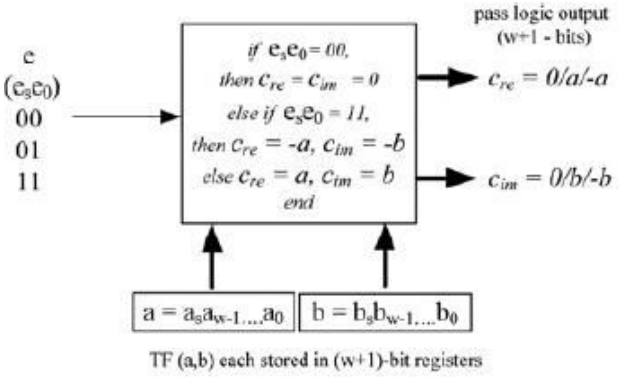


Fig.3 Pass logic

TABLE II
Truth table of the PL

Input (s_0)	Output (w+1) bits	
	c_{re}	c_{im}
00	0	0
01	A	b
11	-a	-b

III. RESULTS AND COMPARISONS

The experimental results of the proposed FFT software architecture are presented in this chapter. Simulation and implementation of FFT with respect to Xilinx ISE 14.2i.are shown.

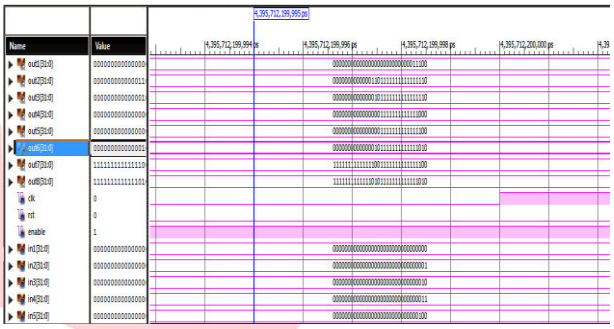


FIGURE 4: SIMULATION RESULT OF 8 POINT FFT WAVEFORM

FIGURE 5: SIMULATION RESULT OF 8 POINT IFFT WAVEFORM

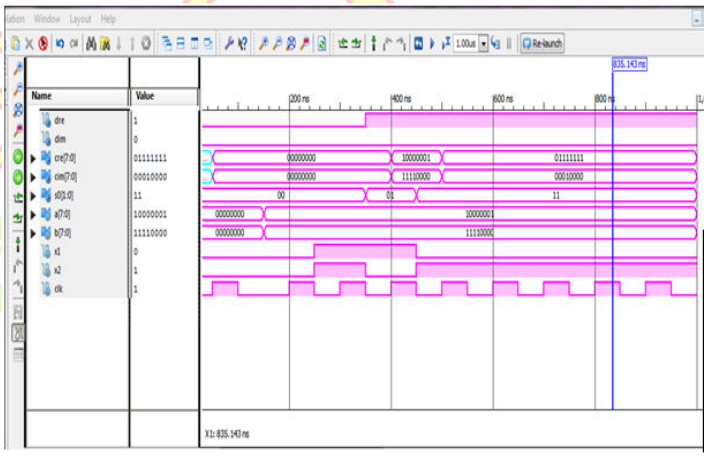
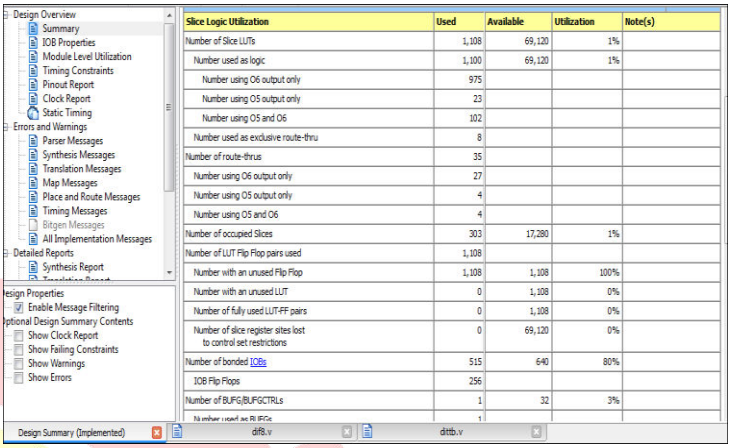


FIGURE 6: PASS-LOGIC WAVEFORM

ISSN 2395-695X (Print)
ISSN 2395-695X (Online)

International Journal of Advanced Research in Biology Engineering Science and Technology (IJARBEST)
Vol. 2, Special Issue 14, May 2016

N-point FFT	No of LUTs utilized	Power(mw)	Delay(ns)
256	1205	1.213	4.966
512	1421	1.209	5.287
1024	1684	1.214	4.199



Slice Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice LUTs	1,108	69,120	1%	
Number used as logic	1,100	69,120	1%	
Number using O6 output only	975			
Number using O5 output only	23			
Number using O5 and O6	102			
Number used as exclusive route-thru	8			
Number of route-thrus	35			
Number using O6 output only	27			
Number using O5 output only	4			
Number using O5 and O6	4			
Number of occupied Slices	303	17,280	1%	
Number of LUT Flip Flop pairs used	1,108			
Number with an unused Flip Flop	1,108	1,108	100%	
Number with an unused LUT	0	1,108	0%	
Number of fully used LUT-FF pairs	0	1,108	0%	
Number of slice register sites lost to control set restrictions	0	69,120	0%	
Number of bonded IOBs	515	640	80%	
IOB Flip Flops	256			
Number of BUFG/BUFGCTRLs	1	32	3%	

FIGURE 8: SYNTHESIS REPORT OF 8 POINT DIF WITH PASS LOGIC

N-point FFT	Type (A)-FFT (B)-FFT with PL	No of LUTs utilized	Total power (mw)
4	(A) (B)	5 4	1.186 1.182
8	(A) (B)	8 6	1.201 1.198
16	(A) (B)	13 11	1.221 1.204

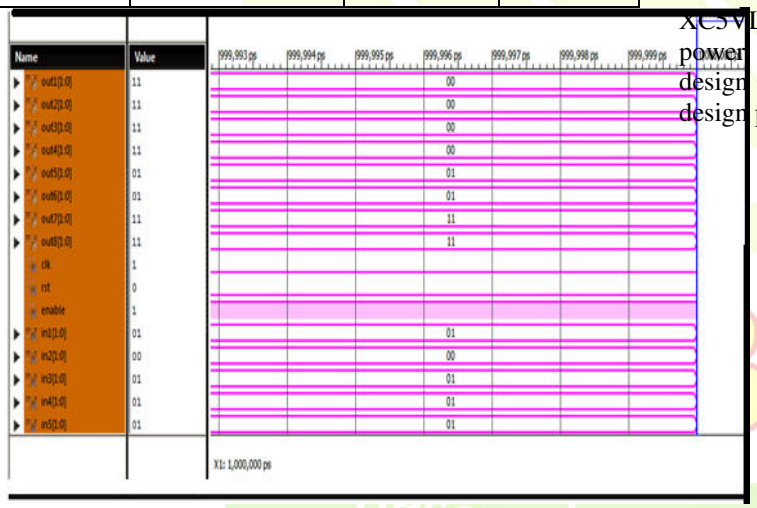


FIGURE 7: 8 POINT FFT WITH PASS LOGIC

The implementation results done on Xilinx Virtex-5, XC5VLX110T and the comparison parameters such as area, power and delay has to be analyzed. Table III shows the design summary of N-point FFT. Table IV compares the design parameter with normal FFT and FFT with pass logic.

TABLE III

DESIGN SUMMARY- COMPARISON OF N-POINT FFT

TABLE IV

COMPARISON OF N-POINT FFT WITH PASS LOGIC

IV. CONCLUSION AND FUTURE ENHANCEMENT

Design of FFT and IFFT was proposed and the FFT algorithm was successfully simulated and tested through Xilinx 14.2i. An 8-point FFT and IFFT with pass logic were computed. This modification reduces the number of multipliers requires in the FFT architecture, in order to reduce area, power and hardware complexity. This is an encouraging phenomenon for high performance OFDM-based wireless communication systems.

ISSN 2395-695X (Print)
ISSN 2395-695X (Online)
International Journal of Advanced Research in Biology Engineering Science and Technology (IJARBEST)
Vol. 2, Special Issue 14, May 2016

REFERENCES

[1] V.Arunachalam, Alex Noel Joseph Raj, (2014) "efficient VLSI implementation of FFT for orthogonal frequency division multiplexing application", IET Circuits Devices Syst., Volume 8,No 6, pp. 526–531

[2] Li, X., Lai, Z., Cui, J.: 'A low power and small area FFT processor for OFDM demodulator (2007)', IEEE Trans. Consum. Electron.,Vol. 53, No.2, pp. 274–277.

[3] Maharatna, K., Grass, E., Jagdhold, U.: 'A 64-point Fourier transform chip for high-speed wireless LAN application using OFDM' (2004), IEEE J. Solid-State Circuits, Vol. 39, No.3, pp. 484–493.

[4] Jiang, H., Luo, H., Tian, J., Song, W.: 'Design of an efficient FFT Processor for OFDM systems' (2005), IEEE Trans. Consum. Electron., Vol. 51, No.4, pp. 1099–1103

[5] Sung, T.-Y., Hsin, H.-C., Cheng, Y.-P.: 'Low-power and high-speed CORDIC-based split-radix FFT processor for OFDM systems', (2010) J. Digit. Signal Process. Vol.20, No.2, pp. 511–527.

[6] Yu, C., Yen, M.-H., Hsiung, P.-A., Chen, S.-J.: 'A low-power 64-point pipeline FFT/IFFT processor for OFDM applications', (2011) IEEE Trans. Consum. Electron., Vol.57, No.1, pp. 40–45.

[7] Jiang, R.M.: 'An area-efficient FFT architecture for OFDM digital video broadcasting', (2007) IEEE Trans. Consum. Electron. Vol.53, No.4, pp.1322-1326

[8] Wu, J., Liu, K., Shen, B., Min, H., 'A hardware efficient VLSI architecture for FFT processor in OFDM systems'. Proc. Sixth Int. Conf. ASIC, Shanghai, China, pp. 232–235,October 2005

[9] Chen, C.-M., Hung, C.-C., Huang, Y.-H.: 'An energy-efficient partial FFT processor for the OFDMA communication system', IEEE Trans. Circuits Syst. II, Express Briefs, Vol.57, No.2, pp. 136–140, 2010

[10] Kim, D.-S., Lee, S.-Y., Chung, D.-J.: 'A partially operated FFT/IFFT processor for low complexity OFDM modulation and demodulation of WiBro in-car entertainment system', IEEE Trans. Consum. Electron., Vol.54, No.2, pp. 431–436, 2008

[11] Jung, Y., Yoon, H., Kim, J.: 'New efficient FFT algorithm and pipeline
Implementation results for OFDM/DMT applications', IEEE Trans. Consum. Electron. Vol. 49, No.1, pp. 14–20, 2003

[12] Cortes, A., Velez, I., Sevillano, J.F., Irizar, A.: 'An approach to simplify the design of IFFT/FFT cores for OFDM systems', IEEE Trans. Consum. Electron. Vol.52, No.1, pp. 26–32, 2006.