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A CASCADED MULTILEVEL INVERTER BASED ON SWITCHED CAPACITOR

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***Abstract*---The objective of the project is to propose inverter topology for multilevel voltage output. This topology is designed based on switched capacitor technique and the number of output level is determined by the number of switched capacitor cells. DC voltage source is used and the problem of capacitor voltage balancing is avoided. The operation and switching sequences are simple when compared to other multilevel inverter topology.The simulation results are validated using MATLAB / SIMULINK. Multilevel inverter outputs were achieved for multiple DC voltage inputs. The output is achieved with Cascaded multilevel inverter based on switched capacitor achieved 9- and 13-levels of voltage output, with a low THD values of 16.11% and 14.41%.**

Keywords: Cascaded H-Bridge, switched capacitor (SC), symmetrical phase shift modulation (PSM), Matlab, and closed loop control.

I INTRODUCTION

The demand for high-voltage high-power inverters is increasing, and it is impossible to connect a power semiconductors switch to a high-voltage network directly. Therefore, multilevel inverters had been introduced and are being developed now. With an increasing number of dc voltage sources in the input side, a sinusoidal like waveform can be generate as the output. As a result, the total harmonic distortion (THD) decreases, and the output waveform quality increases, which are the two main advantages of multilevel inverters is presented in [10]. In addition, lower switching losses, lower voltage stress of dv/dton switches, and better electromagnetic interference are the other most important advantages of multilevel inverters. These kinds of inverters are generally divided into three main categories, i.e., neutral-point-clamped multilevel inverters, flying capacitor multilevel inverters, and cascaded multilevel inverters. There is no diode clamped or flying capacitors in cascaded multilevel inverters is presented in [5]. Moreover, these inverters consist of modularity, simplicity of control, and reliability, and they require the lowest number of power semiconductor devices to generate a particular level. Multilevel inverter technology has emerged recently as a very important alternative in the area of medium voltage energy control. Multilevel inverters include an array of power semiconductors and DC voltage sources is presented in [8], the output of which generate voltages with stepped waveform Comparison with a two-level Voltage-Source Inverter (VSI), the multilevel VSI enables to synthesize output voltages with reduced harmonic distortion and lower electromagnetic interference. By increasing the number of levels in the multilevel inverters, the output voltages have more steps in generating a staircase waveform, which has a reduced harmonic distortion is presented in [6]. However, a larger number of levels increase the number of devices that must be controlled and the control complexity. Now a days there exists three topologies of multilevel inverters. They are Diode clamped, Flying capacitor, Cascaded H-Bridge structure. Moreover, number of capacitors is increased by number of voltage levels.Advantage of multilevel inverter is Soft switching techniques can be used to reduce switching losses and device stresses. Applications of Multilevel inverters have been industrially employed in several applications such as Pump, Fans, Compressors, Photovoltaic power conversion system.

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II. PROPOSED WORK

CIRCUIT EXPLANATION

The proposed circuit is consist of the Switch capacitor frontend and cascaded H-Bridge backend. If the numbers of voltage levels obtained by SC frontend and cascaded H-Bridge backend are N_1 and N2, respectively. Fig.1 represents the circuit topology of nine-level inverter (N1 =2, N2 = 2), where S1, S2, S_1 , S_2 as the switching devices of SC circuits (SC1 and SC2) are used to convert the series or parallel connection of C1 and C2 . S1a, S1b, S1c, S1d, S2a, S2b, S2c, S2d are the switching devices of cascaded H-Bridge. Vdc1 and Vdc2 are input voltage. D1 and D2 are diodes to restrict the current direction. iout and vo are the output current and the output voltage, respectively.

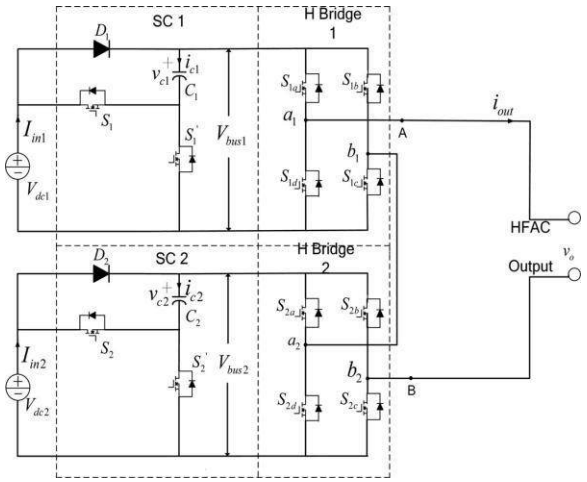
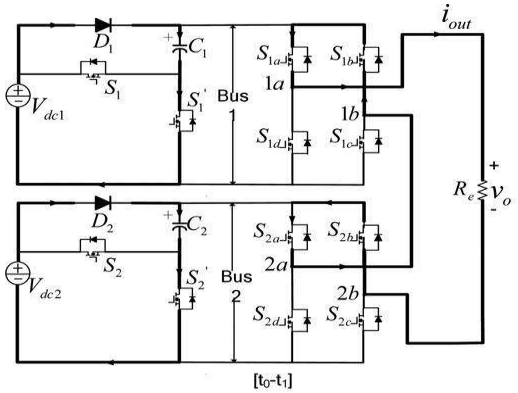


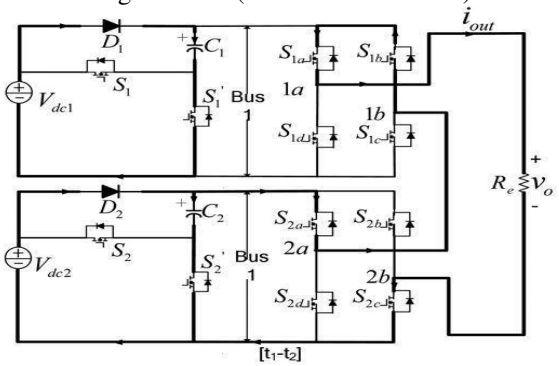
Fig.1. Circuit topology of cascaded nine-level inverter (N1 = 2, N2 = 2).

III. MODES OF OPERATION FOR NINE-LEVEL OUTPUT



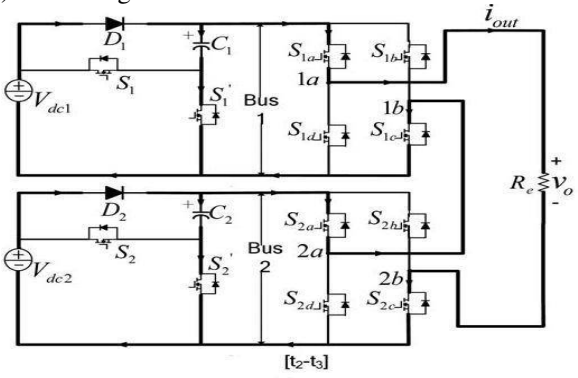
(a)

When t satisfies t0 ≤ t< t1 in Fig.(a), the switches S1a, S1b, S2a, S2b are driven by the gate-source voltage, respectively. H-Bridges 1 and 2 are in freewheeling state, and output voltage equals 0. Because S_1and S_2 are on, the capacitors C1 and C2 are charged to Vin (Vdc1 = Vdc2 = Vin).



(b)

When t satisfies t2 ≤ t < t3 in Fig.(b), the switches S1a, S1c, S2a, S2c are driven by the gate-source voltage, respectively. H-Bridges 1 and 2 are in positive conducting state. Output voltage equals 2*Vin*. Because S_1 and S_2 are on, the capacitors C1 and C2 keep charged to Vin (Vdc1 = Vdc2 = Vin).The voltages on Bus 1 and Bus 2 are Vin as well.



(c)

When t satisfies t3 ≤ t < t4 in Fig. (c), the switches S1a, S1c, S2a, S2c are driven by the gate-source voltage, respectively. H-Bridges 1 and 2 are in positive conducting state. Output voltage equals 3Vin . Because *S*_1 and *S*2 are on, the capacitor *C*1 keeps charged to Vin (Vdc1 = Vdc2 = Vin), and the capacitor C2 is discharged. The voltages on Bus 1 and Bus 2 are Vin and 2Vin ,respectively.

When t satisfies t4 ≤ t < t5 in Fig.(d), the switches S1a, S1c, S2a, S2c are driven by the gate-source voltage, respectively. H-Bridges 1 and 2 are in positive conducting state. Output voltage equals 4*Vin*. Because *S*1 and *S*2 are on, the capacitor *C*1 and *C*2 are discharged. The voltages on Bus 1 and Bus 2 both are 2*Vin* .

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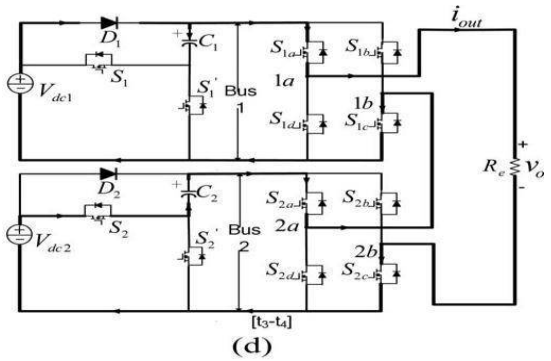
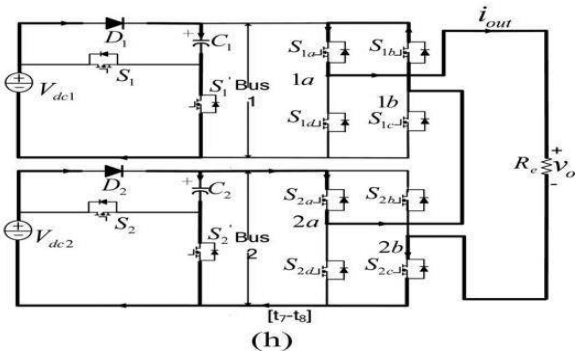
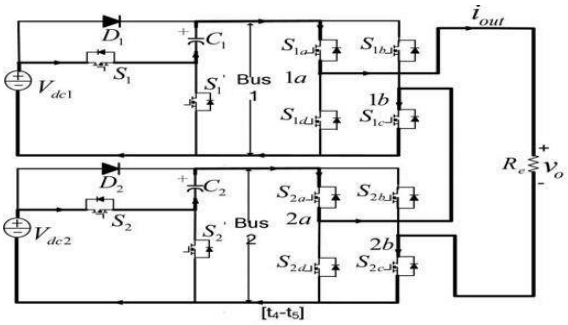


(d)

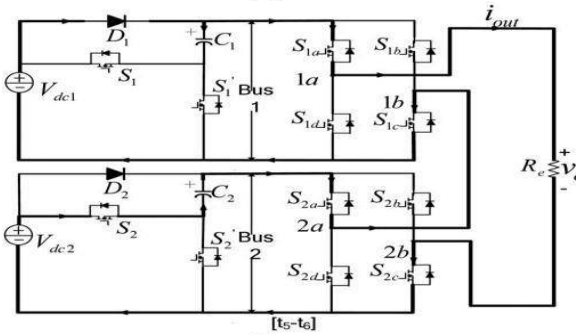


(h)

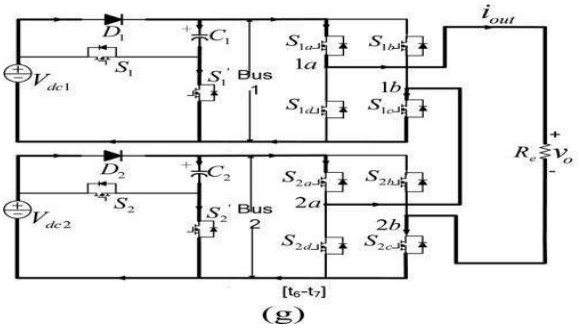
The operations in t5 ≤ t < t6, t6 ≤ t < t7 , and t7 ≤ t < *t*8, are the same as the operations in t3 ≤ t < t4, t2 ≤ t < t3 , and t1 ≤t< t2 , respectively.



(e)



(f)



(g)

IV. TABULATION

On-state switches	Output voltage	Capacitor State
S_{1a}, S_{1c}, S_{2a}, S_{2c}, S_1,S_2	$4V_{in}$	C_1, C_2 Discharging
S_{1a}, S_{1c}, S_{2a}, S_{2c}, S_1', S_2	$3V_{in}$	C_2 Discharging
S_{1a}, S_{1c}, S_{2a}, S_{2c}, S_1' S_2'	$2V_{in}$	C_1, C_2 Charging
S_{1a}, S_{1b}, S_{2a}, S_{2c}, S_1' S_2'	V_{in}	C_1, C_2 Charging
S_{1a}, S_{1b}, S_{2a}, S_{2b}, S_1' S_2' or S_{1c}, S_{1d}, S_{2c}, S_{2d}	0	C_1, C_2 Charging
S_{1c}, S_{1d}, S_{2b}, S_{2d}, S_1' S_2'	$-V_{in}$	C_1, C_2 Charging
S_{1b}, S_{1d}, S_{2b}, S_{2d}, S_1' S_2'	$-2V_{in}$	C_1, C_2 Charging
S_{1b}, S_{1d}, S_{2b}, S_{2d}, S_1', S_2	$-3V_{in}$	C_2 Discharging
S_{1b}, S_{1d}, S_{2b}, S_{2d}, S_1,S_2	$-4V_{in}$	C_1, C_2 Discharging

Table – a. Switching sequences

V. PARAMETERS

SI.NO	PARAMETERS	9-LEVEL	13-LEVEL
1	SC	4	6
2	Diodes	2	3
3	Capacitor	2	3
4	H-Bridge	2	3
5	DC-source	2	3
6	Input voltage	200	300
7	Output voltage	100	600
8	THD	16.11	14.41

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VI. SIMULATION RESULTS

A.Simulation circuit for nine level inverter

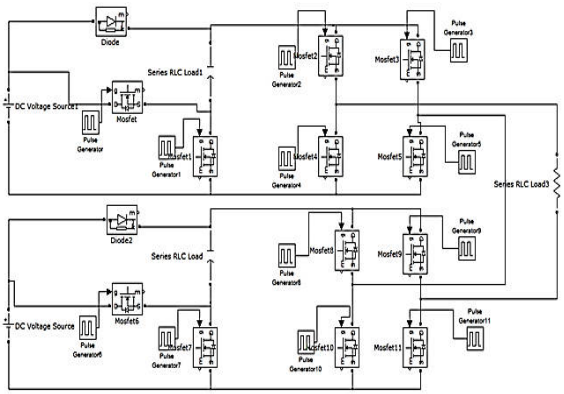

Fig.2.Simulink diagram for nine level inverter

Figure 2 shows the total harmonic distortion of above nine level inverter figure 2 at fundamental frequency 50Hz and observed total harmonic distortion is 16.11%. It is to be noted that, Junfeng Liu et al. (2014) reported a THD value of 19.1% for the same nine–level inverter topology.

B. Nine level output inverter voltage waveform

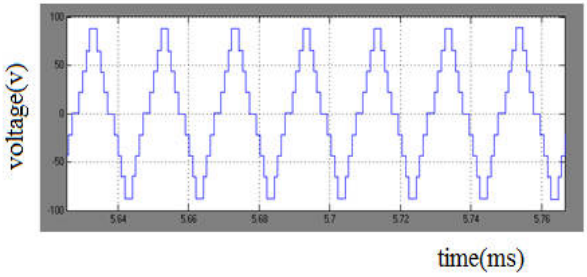

Fig.3.Nine level output inverter voltage waveform

C. Total harmonic distortion

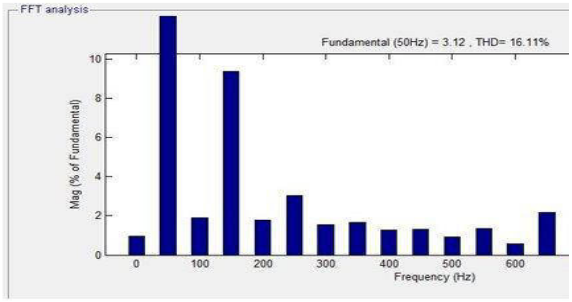

Fig.4.Total harmonic distortion

D. Simulation circuit for thirteen level inverter

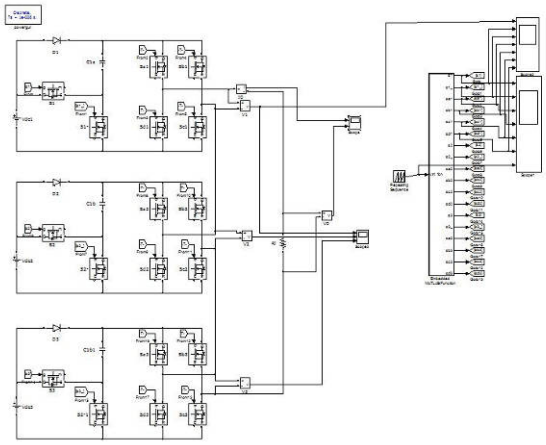

Fig.5.Simulink for thirteen level inverter

E. Thirteen level output inverter voltage waveform

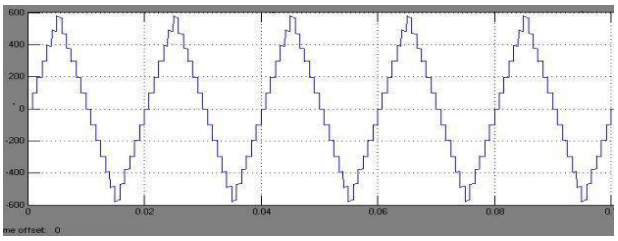

Fig.6.Thirteen level output inverter voltage waveform

F. Total harmonic distortion

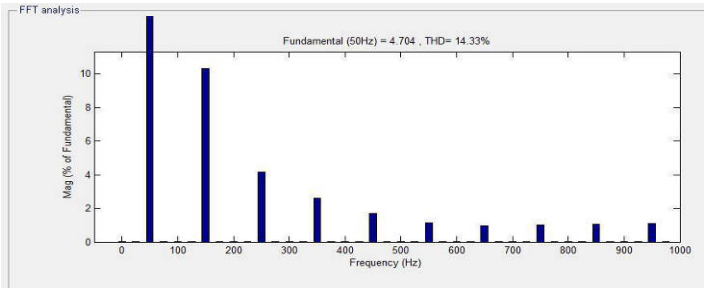

Fig.7.Total harmonic distortion

CONCLUSION

A multilevel inverter with switched capacitor topology has been simulated to obtain 9- and 13-level inverter output with multiple DC input voltages. The proposed topology uses multiple DC voltage source and the problem of capacitor voltage balancing is avoided. The proposed topology uses a PWM coding

techniques as compared to the reported similar topology (Liu et al. 2014), and are able to reduce the THD value in the 9-level multilevel inverter output to 16.11% from 19.11% reported in the literature. This structure is simple and easily can be extended to higher levels. Cascaded multilevel based on switched capacitor achieved 9- and 13-levels of voltage output, with a low THD values of 16.11% and 14.41%, respectively.

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