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A Well-Configured 3-bit & 4-bit Hybrid Modified Booth Multiplier

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***Abstract*— This paper presents a High-Level Design methodology for high-speed/low-power Modified Booth Multiplier (MBM) by altering its basic Modified Booth Encoding (MBE) scheme. Instead of 3-bit pair recoding, new re-modified booth use 3 and 4-bit pair hybrid encoding scheme for the reduction of partial product generation and to improve the performance/speed of the multiplication process. The 0.25 µm scale Re-Modified Booth scheme gives 11.7% of power reduction while comparing with basic MBM.**

Keywords-High level design, Low-power, Modified booth multiplier, Bit-pair recording.

I. INTRODUCTION

The increasing prominence of portable systems and the demand to limit power consumption in very-high density VLSI chips have led to rapid and innovative developments in low-power design throughout the current years. The requirements of low-power consumption must be met along with equally demanding goals of high chip density and high throughput. Hence, low-power design of digital integrated circuits has emerged as a very active and rapidly developing field of CMOS design.

The methodologies which are used to achieve low-power consumption in digital systems span a wide range, from device/process level to algorithm level. Device characteristics (e.g., threshold voltage), device geometries and interconnect properties are significant factors in lowering the power consumption. Circuit-level measures such as the proper choice of circuit design styles, reduction of the voltage swing and clocking strategies can be used to reduce power dissipation at the transistor level. Architecture-level measures include smart power management of various system blocks, utilization of pipelining and parallelism, and design of bus structures. Finally, the power consumed by the system can be reduced by a proper selection of the data processing algorithms, specifically to minimize the number of switching events for a given task.

As well as need for low-power design is becoming a major issue in high-performance digital systems, such as microprocessors, Digital Signal Processors (DSPs) and other applications. Multiplication is a fundamental operation in most signal processing algorithms. Multipliers have large area, long latency and consume considerable power. Therefore, low-power multiplier design has been an important part in low-power VLSI system design. There has been extensive work on low-power multipliers at technology, physical, circuit and logic levels. This paper addresses high-level design techniques for low power multipliers to reduce its switching activities. High-level techniques refer to algorithm and architecture level techniques that consider multiplication's arithmetic features and input data characteristics.

The main research idea of this work is how to optimize the internal algorithm and architecture of multipliers and how to control active multiplier resource to match external data characteristics. The primary objective is power reduction with delay overhead. By using new algorithms or architectures, it is even possible to achieve both power reduction and delay reduction, which is another strength of high-level optimization. The tradeoff between power and delay is also considered in some cases.

II. LITERATURE SURVEY

Multiplication can be well thought-out as a series of repetitive additions. The number to be added is the multiplicand, the number of times that it is added is the multiplier, and the result is the product. Each stair of the addition generates a partial product. In most computers, the operands habitually contain the similar number of bits. When the operands are interpreted as integers, the product is generally twice the length of the operands in order to preserve the information content. This repeated addition method that is suggested by the arithmetic definition is slow that it is almost always replaced by an algorithm that makes use of positional number representation.

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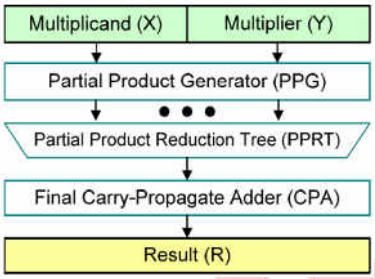

Fig.(1). The block diagram of a MBM [13]

It is possible to decompose multipliers in two parts. The first part is dedicated to the generation of partial products, and the second one collects and adds them. As for adders, it is possible to enhance the intrinsic performances of multipliers. Acting in the generation part, the Booth (or modified Booth) algorithm is often used because it reduces the number of partial products. The collection of the partial products can then be made using a regular array, a Wallace tree or a binary tree or a carry propagation adder as shown in the fig.1.

Many prior digital multipliers were aimed at transition or switch reductions to diminish power dissipation. The power reduction method used in a MBM is the 3-bit pair recoding scheme [1]. This 3-bit MBE has been widely used in parallel multipliers to reduce the number of partial products by a factor of two. A proof of MBE has been given in [2] and the major disadvantage of the algorithm is that the process still requires n shifts and an average of n/2 additions for an n bit multiplier. In [3]-[7], the speed performance of using radix-4 MBE was denied. However, the increasing capacitive wire load and operands' bit length result in very large power dissipation, [8]-[12].

A technique that reduces number of full adders in the compression tree of signed/unsigned MBA is described in [9] also it is based on the need to extend the sign bit of the partial products. A multiplexer, F-Block and adder-cum-subtractor module is used for the 625.2 MH_z, 2µm scale NMOS parallel implementation of 4x4 bit MBA is in [10] with an area of 1.37 mm^2 and based on the extension of 2^{nd} order MBA novel concurrent carry save multiplier accumulator (MAC) architecture is revealed in [11] with different computational performance. A new encoding scheme with multiple-level conditional-sum adder (MLCSMA) hybrid structure has been proposed in [12] to improve the performance up to 25% in booth encoded parallel multiplier design. A rearranging and reducing partial products to achieve an extra-row-removal for the multiplier is possible by [13] with a hybrid spare-tree structure is used in designing two's complementation circuit which further reduce the area to 15.8% and improve the speed up to 11.7% over the classical design. In [15] the booth multiplier is compared against Radix-4 and Multiplication Algorithm for Switching Activity Reduction (MASAR) multipliers through Operand Decomposition [16]-[19] in terms of power dissipation, area and delay with a conversion from Redundant Binary Signed Digit (RBSD) to standard binary (SB) form has been present. It is found herein that these results depend on the implementation of MBE scheme.

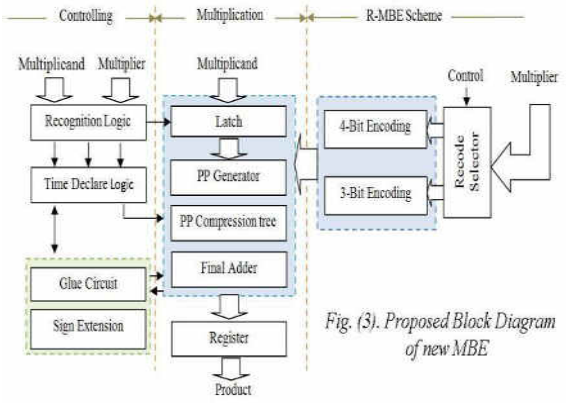

Fig. (3). Proposed Block Diagram of new MBE

The proposed block diagram of MBM with a hybrid scheme is shown in the fig.(3). In the block diagram, 3 and 4-bit hybrid coding technique is planned with the MBM.. Also a Recognition Logic with Timing declaring circuit has been given to the hybrid technique to precisely operate the device to get reduces the power. A glue circuit has been recommended to control the carry and a sign extension circuit which will perfectly manage the sign of the product also proposed.

4- Bit Group	Code	Operation
0000	0	Add 0 to *PP**
0001	1	Add *M*** to *PP*
0010	2	Shift *M* left by 1 bit and add to *PP*
0100	3	Shift *M* left by 2 bit and add to *PP*
1000	4	Shift *M* left by 3 bit and add to *PP*
0011, 0101 to 0111, 1001 to 1111	3-Bit MBE Scheme	

* *Partial Product* ** *Multiplicand*

Table (1). 4-Bit Encoding Scheme

Consider a Modified Booth Multiplication with two numbers "0101011100101101" and "0000001011010100". From the above table (1) the Hybrid Bit Pair Recoding of multiplier "0000001011010100" can be written as shown in the fig. (2). Here both 3 and 4-bit recoding scheme is used to find out the encoded bit. Like normal 3 bit recoding scheme there is no virtual zero at the LSB of the multiplier for encoding in 4-bit. If the encoding can be done with 4-bit we can reduce the 4 number of partial product into one PP, otherwise we should go for normal 3-bit encoding scheme. So it is called 3 and 4-bit Hybrid recoding scheme.

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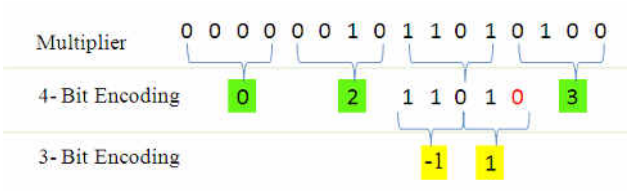

Fig. (2). Example of the 3 & 4-Bit Hybrid Encoding Scheme.

The recoded output '02-113' has been considered as new multiplier and this will reduce the multiplication process from its original step, if we are using Hybrid encoding scheme the production of PP can be reduced to a certain limit. In the example fig. (4). Shows only five PP is enough to solve the problem instead of eight PP in 3-bit MBE scheme.

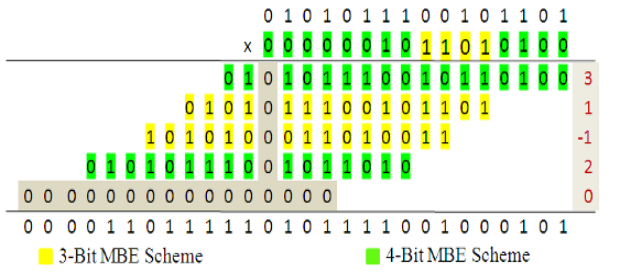

Fig. (4). 3 & 4-Bit Hybrid Multiplication Scheme.

The MBE PP candidates are generated by MUX or logic elements. The output of MBE is fed to a carry look ahead adder for to compress the partial product, to reduce switching power and to get the final result. The carry-look ahead adder can be broken up in two modules: (1) the Partial Full Adder (PFA),which generate sum and (2) the Carry Look-ahead Logic which generate the carry out bit The block diagram representation of a 4-bit carry look ahead adder has been shown in the fig.(5) and it's schematic is shown in fig.(7).

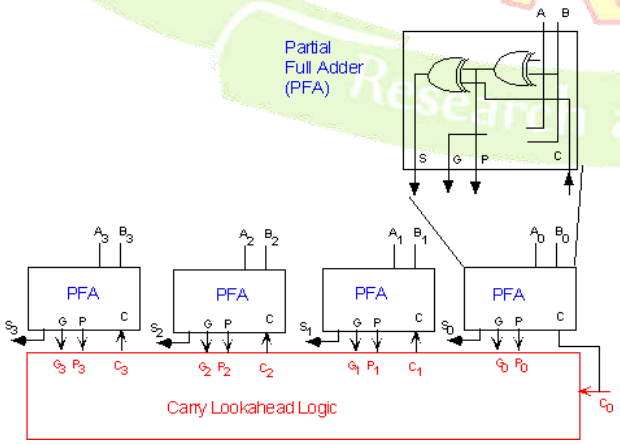

Fig.(5) 4-bit Carry Look Ahead adder logic

IV. PERFORMANCE EVALUATION AND COMPARISON

The Re-Modified booth multiplier design has been realized by following the standard cell-based design flow with an in-house CMOS cell library in Tanner EDA 12.6 tool. This design is verified via transistor-level simulation in 0.25µm scale. Fig. (6) Shows the proposed Re-Modified Booth Multiplier layout diagram.

Furthermore, we measure the power dissipation of the three multipliers (normal multiplication, Booth Multiplication and R-MBE) in terms of different bit ranges, i.e. 16-bit, 32-bit, and 64-bit. The simulation results are shows R-MBE consume less power than other multipliers as shown in table (2).

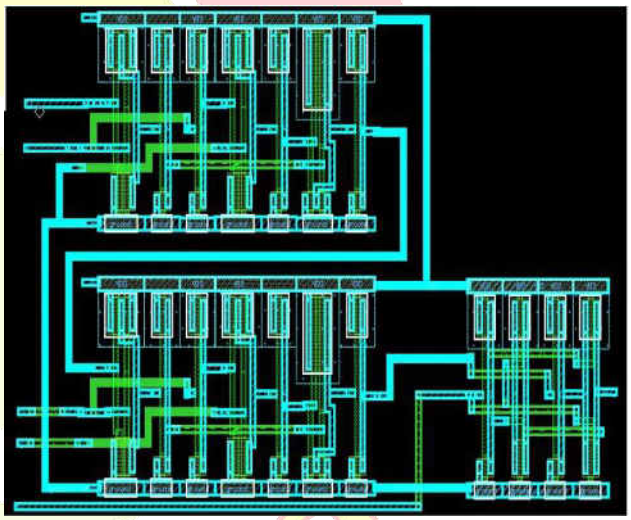

Fig.(6). Layout diagram of Hybrid MBE

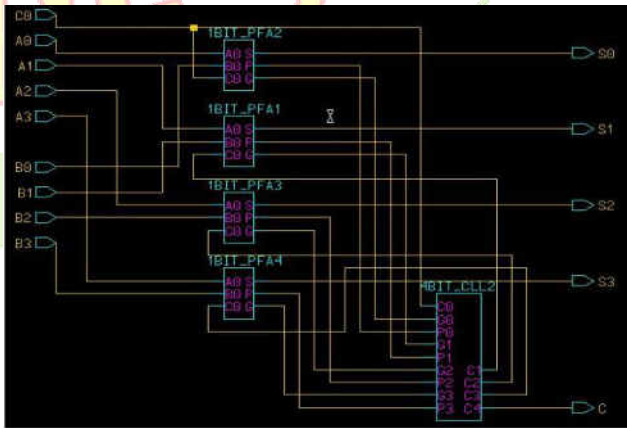

Fig.(7). Schematic diagram of 4-bit Look Ahead Adder

This high level approach of multiplication will give power reduction as well as area reduction as shown in the table (2).

Design	Power/MHz	Area (Tr.)
Normal M*	0.0991	1454
MBE[ed] M*	0.0411	1031
R-MBE[ed] M*	0.0368	1018

*Multiplication

Table (2). *Simulation Results of Three Multipliers*

V. CONCLUSION

In this paper, we have presented a well-configured MBE multiplier design. The design is well-structured because an improved 4-bit modified Booth encoder without an implied zero is used. So that rearranging and reducing partial products to achieve and row-removal for the multiplier is possible. Hybrid structure of 3-bit and 4-bit coding is used to designing circuit which reduce the area and improve the speed. This multiplier architecture is implemented in 0.25 µm scale Tanner EDA tool. According to the experimental results, the design can obtain 9.8% and 11.7% on the area and power savings respectively over the classical design and 7.5% and 5.5% area and power saving respectively over the design [14] which was reported to give the best performance.

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