Design and implementation of reversible carry look ahead adder and array multiplier

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Abstract— **Reversible logic is a leading area in the quantum computing study. Less number of garbage outputs, decreased quantum cost and reduced power dissipation are the motives for reversible logic. Proper utilization of logical reversibility can have good results only after employing physical reversibility. For the optimization of quantum cost, gate count and power dissipation we have used properties of Peres gate, MHNG gate, TKS gate for both carry look ahead adder and array multiplier. The implemented logic designs are simulated using Xilinx 14.2 and RTL compiler is used to synthesize a proposed design.**

Keywords- Reversible logic, Reversible gates, Quantum cost

I. INTRODUCTION

R. Launder stated that a conventional irreversible circuit has some energy loss resulting in information loss. In 1973, Bennett presented a theory stating that loss of information can be reduced by using the reversible circuit components. Reversible logic has its origin in the concepts of Quantum Computing. The conventional circuit dissipates KTlog2 Joules of energy for every bit to last, irrespective of the design configuration used. The design which results in no information loss is said to be reversible. In a system using reversible configuration, the system has no information loss and it dissipates a very small amount of energy KT Ln (1) which is zero. These are the generalized form of conventional logic gates. It has n number of inputs and n number of outputs, there exist a one to one mapping. It allows the recreation of the input vector from outputs and we can determine the inputs from the generated outputs [1-3].
There are two reversible cases possible:-

1. A device is called reversible if its input and output can be uniquely retrieved from each other and is called logical reversibility.
2. A device that can run in the backward direction is called physically reversible.

Feedback paths are not allowed, i.e. circuit is acyclic. For the design of an ideal reversible circuit, the number of constant inputs, garbage outputs, and the reversible gate should be kept the minimum [4-6].

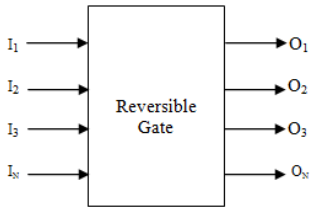


Fig.1 General Reversible Gate

II. REVERSIBLE GATES

The reversible gate is of many types, but here for the purpose we are using TKS gate, Peres gate, and MHNG gate. Working on TKS gate, Peres gate and MHNG gate are stated below [7].

A. TKS GATE

TKS gate is a 3x3 type gate having 3 inputs (A, B, C) and 3 outputs (P, Q, R). It can be used to implement any Boolean expression because two of its outputs (P & R) can work as 2:1 multiplexer.

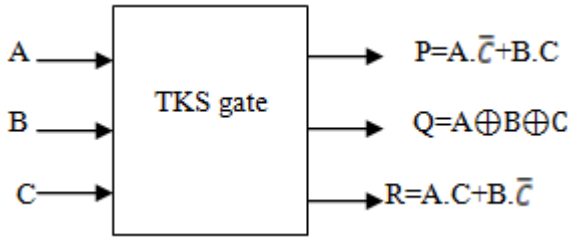


Fig.2.1 TKS Gate

B. Modified HNG Gate:

The modified HNG gate is a 4x4 logic gate having 4 inputs (A, B, C, D) and 4 outputs(P, Q, R, S). The MHNG gate provides functionality that it can be used as a single unit of a full adder and a half adder. For full adder input configuration will be A, B, C_{in}, 0 and output configuration will be A, 0, Sum, C_{out}. And for half adder inputs configuration will be 0, B, C_{in}, 0 and output configuration will be 0,0, Sum, C_{out} [8].

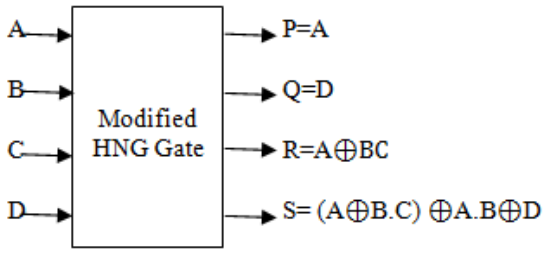


Fig.2.2 Modified HNG Gate

C. *Peres Gate*

Peres gate is a 3x3 type gate. It has 3 inputs (A, B, C) and 3 outputs (P, Q, R) as shown in fig.2.3. For designing of both carry look ahead adder and array multiplier Peres gate is most suitable because it has low quantum cost of 4.

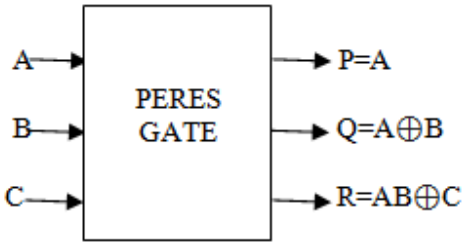


Fig.2.3 Peres Gate

III. CARRY LOOK AHEAD ADDER

The addition is the most used binary operation because each arithmetic operation is performed by successive addition. A conventional binary adder is not speed efficient because when adding two numbers its speed is directly proportional to carry generated during operation. Speed/Time delay reduction in a physical circuit is limited to their capacity. The Carry Lookahead adder is one of the several methods to reduce delays caused due to carry.

In Carry look ahead adder faster technique is used to calculate future carry in advance. And we can make this Carry look ahead adder, even more, energy efficient by using reversible configuration. For designing above mentioned reversible Carry look ahead adder unit we have used properties of Peres gate and TKS gate [9-11]. First, we have designed a block to calculate carry in advance which is comprised of the Peres gate as shown in fig.3.1.

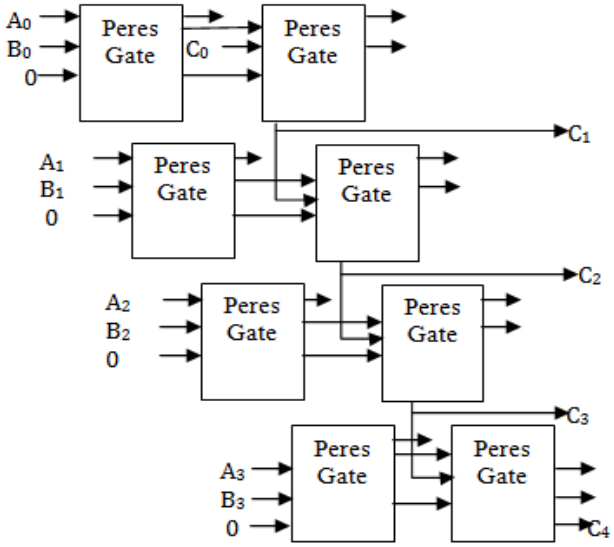


Fig.3.1 Circuit for generation of carry Signals

Thus, from the above circuit by using Peres gate we have calculated C_1, C_2, C_3 C_4 (C_{out}). Now we will calculate the sum for two 4-bit numbers using TKS gate. For the result of the sum we need to implicate an expression of $A_i \oplus B_i \oplus C_i$ which we can be implemented by the TKS gate as we know the second output of TKS gate gives the same expression which we need for Sum of Carry look ahead adder. Circuit design for Sum is shown in fig 3.2.

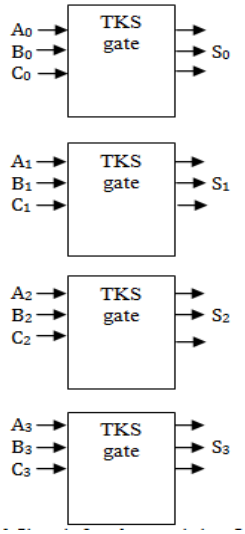


Fig.3.2 Circuit for determining Sum output

IV. Reversible Array Multiplier

Digital multiplication is the most extensively used operations. Digital signal processing is the most prominent area where multiplication is used.

We have designed array multiplier using reversible gates to increase performance. In this reversible array multiplier number, constant inputs and garbage outputs are less which is essential for efficient quantum calculations [12-14]. For determining partial product we have used an array of Peres gate as shown in fig.4.1 and for the addition of partial product, we need full adders and half adders to be implemented in reversible fashion. To implement full adder and half adders we can use MHNG gate in different configurations.

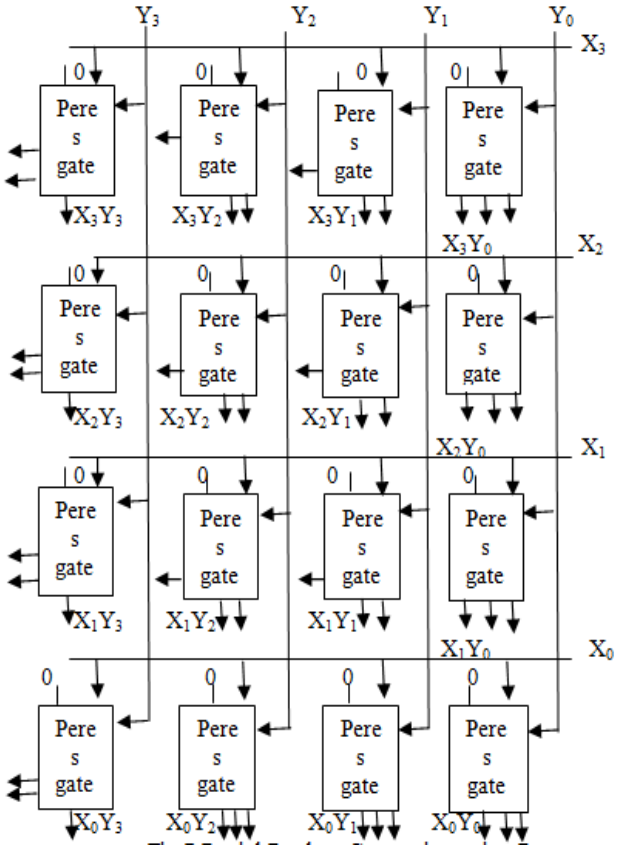


Fig.4.1 Generation of Partial Products using Peres Gate

For the purpose of final product, we have used MHNG gate to design full adder but to design half adders we have used Peres gate to reduce the complexity of the circuit [15-16]. Along with the reduction in complexity, we have used garbage output (zero) produced by MHNG gate as input for the next gate.

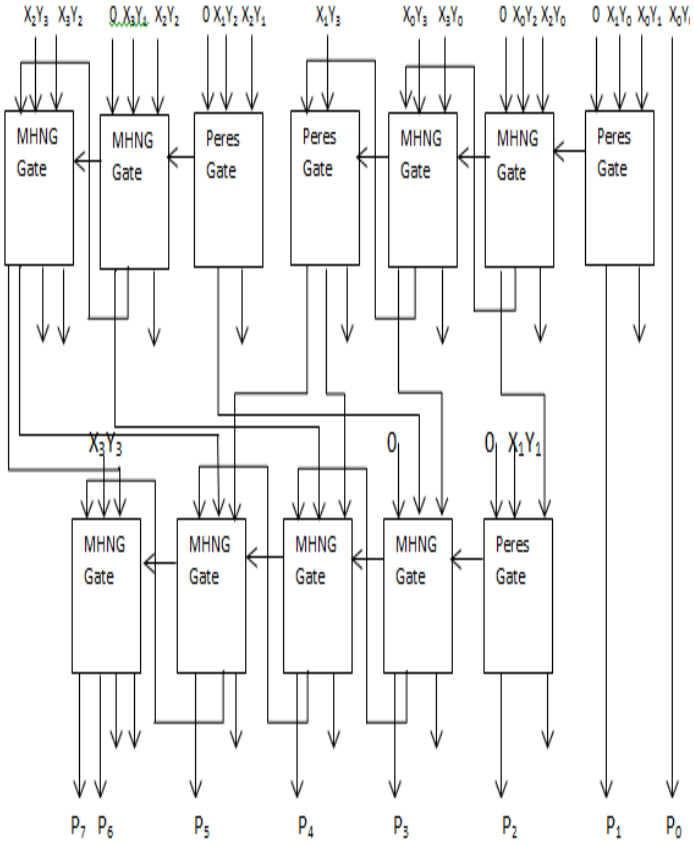


Fig.4.2 Final product generation

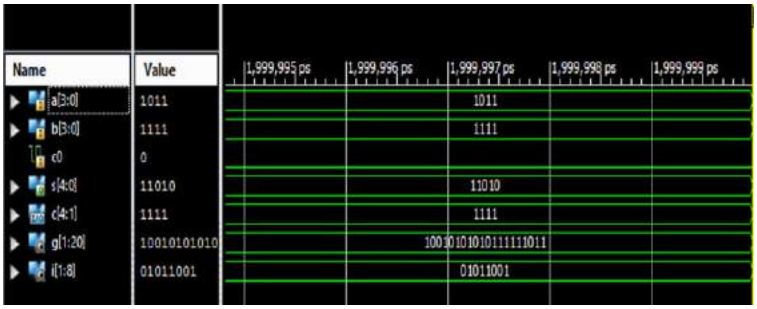
V. Simulation Results

Above derived reversible Carry Look Ahead Adder and reversible array multipliers are simulated using Xilinx 14.2 Simulation results shown in below for both.

A. Carry look ahead adder

Simulation report data for utilization is as shown below

Number of Slices:	4 out of	960	0%
Number of 4 input LUTs:	8 out of	1920	0%
Number of IOs:	18		
Number of bonded IOBs:	18 out of	66	27%



Fag.5.1 Simulation results for carry look ahead adder

B. Array Multiplier

Simulation report data for utilization is as shown below

Number of Slices:	18 out of	4656	0%
Number of 4 input LUTs:	32 out of	9312	0%
Number of IOs:	16		
Number of bonded IOBs:	16 out of	232	6%

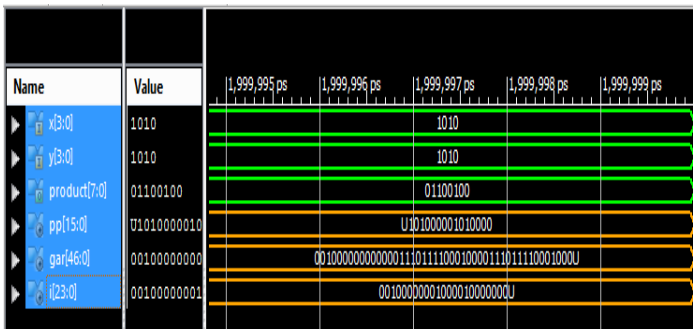


Fig.5.2 simulation results for Array Multiplier

VI. CONCLUSION

In this paper, we have designed an 8-bit reversible carry look ahead adder and array multiplier using Peres gate, TKS gate, MHNG gate which results in a decrease in the number of constant inputs and garbage outputs. An area used by reversible circuits is less than conventional circuit due to which cost decreases. In terms of efficiency, the reversible circuit is more efficient and speed of operation is also better than conventional circuits. Along with the less garbage output, the constant input reversible circuit is helpful in the efficient quantum calculation.

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