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“SRAM”DESIGN OF LOW SUPPLY VOLTAGE IN LEAKAGE COMPENSATION AND READ DELAY COMPENSATION

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***Abstract*— A leakage current compensation design for nano scale SRAMs is proposed in this paper. The proposed SRAMs cell is implemented with transmission gate. A current mode sense amplifier which is proved to achieve low power and high speed is presented. Its sensing delay is independent of the capacitances. Its sensing delay and power consumption are almost independent of the bit- and data-line capacitances. In the proposed SRAM topology, additional circuitry has been added to a standard 5T-SRAM cell to improve the static noise margin (SNM) and the performance. At 0.6 V system voltage, the read delay is reduced 54.88% the proposed compensation design reduces 27.86% of the average power dissipation. The proposed Static Random-Access Memory is implemented using the TSMC 40-nm CMOS logic technology. It is reduces the power consumption and read delay.**

***Index Terms*— Compensation circuit, disturbfree, leakage curent sensor, Static Random-Access Memory cell, SRAM.**

I. INTRODUCTION

SRAM has been an important role in many products, e.g., the cache of CPU. SRAM is faster and more expansive .Show the fig 1 CMOS with SRAM. A typical SRAM cell is made up of six MOSFETs. Each bit in an SRAM is stored on four transistors M1, M2, M3, M4 that form two cross coupled inverters. This storage cell has two stable states which are used to denote 0 and 1. Two additional transistors serve to control the access to a storage cell during read and write operations.

In addition to such six-transistor 6T SRAM, other kinds of SRAM chips use 4, 8, 10 4T, 8T, 10T SRAM, or more transistors per bit. Four-transistor SRAM is quite common in stand-alone SRAM devices as opposed to SRAM used for CPU caches, implemented in special processes with an extra layer of polysilicon, allowing for very high-resistance pull-up resistors. The principal drawback of using 4T SRAM is increased static power due to the constant current flow through one of the pull-down transistors.

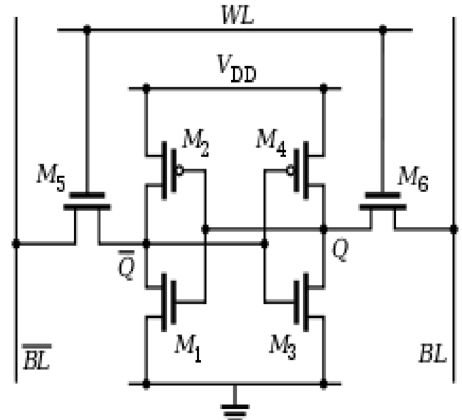

Fig.1 CMOS with SRAM

sometimes used to implement more than one read and/or write port, which may be useful in certain types of video memory and register files implemented with multi-ported SRAM circuitry. Generally, the fewer transistors needed per cell, the smaller each cell can be. Since the cost of processing a silicon wafer is relatively fixed, using smaller cells and so packing more bits on one wafer reduces the cost per bit of memory.

Memory cells that use fewer than four transistors are possible but, such 3T or 1T cells are DRAM, not SRAM even the so-called 1T-

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SRAM. Access to the cell is enabled by the word line WL in figure which controls the two transistors M_5 and M_6 which, in turn, control whether the cell should be connected to the bit lines: BL and BL. They are used to transfer data for both read and write operations. Although it is not strictly necessary to have two bit lines, both the signal and its inverse are typically provided in order to improve noise margins.

During read accesses, the bit lines are actively driven high and low by the inverters in the SRAM cell. This improves SRAM bandwidth compared to DRAMs in a DRAM, the bit line is connected to storage capacitors and charge sharing causes the bit line to swing upwards or downwards. The symmetric structure of SRAMs also allows for differential signalling, which makes small voltage swings more easily detectable. Another difference with DRAM that contributes to making SRAM faster is that commercial chips accept all address bits at a time. By comparison, commodity DRAMs have the address multiplexed in two halves, i.e. higher bits followed by lower bits, over the same package pins in order to keep their size and cost down.

To extend the operation time and reduce power dissipation, Static Random-Access Memory (SRAM) is usually fabricated using advanced processes. SRAM is a type of semiconductor memory. The on chip memory support circuitry implements read/write functions.

1) SRAM operation

SRAM operating in read mode and write modes should have "readability" and "write stability", respectively. The three different states work as follows:

a) Standby

If the word line is not asserted, the access transistors M_5 and M_6 disconnect the cell from the bit lines. The two cross-coupled inverters formed by M_1 – M_4 will continue to reinforce each other as long as they are connected to the supply.

b) Reading

Reading only requires asserting the word line WL and reading the SRAM cell state by a single access transistor and bit line, e.g. M_6, BL. Nevertheless, bit lines are relatively long and have large parasitic capacitance. To speed up reading, a more complex process is used in practice: The read cycle is started by precharging both bit lines BL and BL, i.e., driving the bit lines to a threshold voltage midrange voltage between logical 1 and 0 by an external module. Then asserting the word line WL enables both the access transistors M_5 and M_6, which causes the bit line BL voltage to either slightly drop (bottom NMOS transistor M_3 is ON and top PMOS transistor M_4 is off or rise top PMOS transistor M_4 is on.

c) Writing

The write cycle begins by ap plying the value to be written to the bit lines. If we wish to write a 0, we would apply a 0 to the bit lines, i.e. setting BL to 1 and BL to 0. This is similar to applying a reset pulse to an SR-latch, which causes the flip flop to change state. A 1 is written by inverting the values of the bit lines. WL is then asserted and the value that is to be stored is latched in. This works because the bit line input-drivers are designed to be much stronger than the relatively weak transistors in the cell itself so that can easily override the previous state of the cross-coupled inverters.

II. OPTIMAL SIZING FOR SRAM CELL

The structure of the Existing SRAM using the leakage current sensor and the compensation circuit is shown in Fig.2.

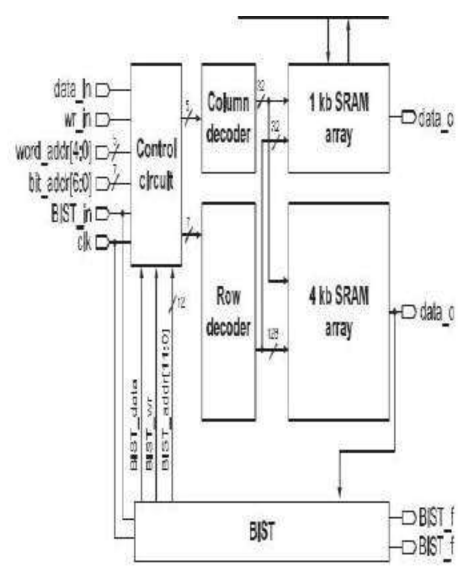

Fig.2 Block Diagram of SRAM.

SRAMs contribute to a significant portion of the total power dissipation. SRAMS usually support read and write operation. The compensation circuitry, two SRAM arrays arrays are carried on the same die sharing common row decoder and column decoder the 1-kb SRAM array with compensation only needs bit_addr, while the 4-kb SRAM array without compensation needs bit_addr. A control circuit includes several MUXs, which allow BIST_in to select either the normal operation mode or the build-in-self-test (BIST) mode. wr_in determines the entire SRAM is the read mode (wr_in = logic 1) or the write mode (wr_in = logic 0), respectively. word_addr and bit_addr drive column and row decoders to select the corresponding cell, respectively.

1) ANALYTICAL MODELS FOR SRAM LEAKAGE CURRENT

The objective of this work is to develop models parameterized in terms of high level design parameters. As indicated in Section 3, SRAMs are primarily composed of 6 sub-blocks: memory-core, address decoder, read column circuit, write column circuit, read control and write control circuit. We consider the typical implementation styles of these sub-blocks and develop leakage power models for each sub-block in each of its operational phase (read, write, precharge, and idle). To simplify the analysis, we assume that the leakage current in a sub-block during a transient state is same as the leakage current when it reaches a steady state. Although this approximation might introduce some error, we show in Section 6 that the error margin is reasonable.

2) 8T SRAM Cell

8T SRAM cell with stack forcing in pull down NMOS circuits shown in Fig.3.By using another higher supply voltage, the access of the SRAM cell will be fastened. For example, by boosting the bit line voltage, the write speed can be improved due to the current of the access transistor is increased. By contrast, by boosting the supply voltage and reversing body bias voltage in the 6T SRAM cell, the leakage reduction is better than the 8T SRAM cell with stack forcing in pull-down NMOS.

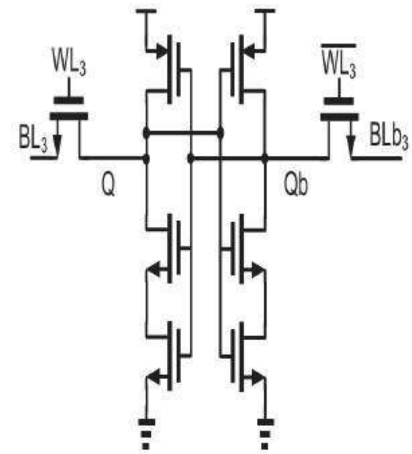

Fig. 3 8T SRAM Cell With Stack Forcing in Pull-Down nMOS

III 5T SRAM WITH TRANSMISSION GATE LEAKAGE SENSOR AND READ DELAY COMPENSATION

A transmission gate is similar to a relay that can conduct in both direction or block by a control signal with almost any voltage potential. It is CMOS based switch in which PMOS passes a strong 1 but por0 and NMOS passes strong 0but poor 1.Both PMOS and NMOS work simultaneously.

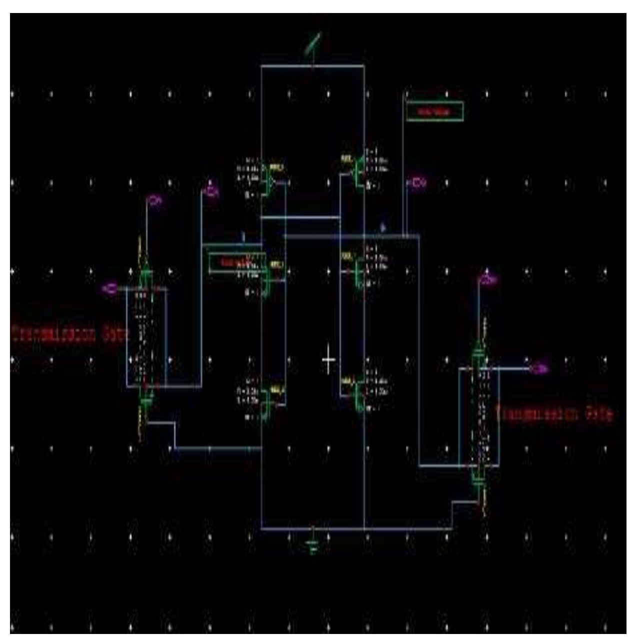

Fig.4 proposed 5T SRAM with transmission gate.

Fig.4 shows the proposed 5T SRAM with transmission gate. The proposed compensation design is composed leakage current sensor and compensation circuit. A novel five transistor SRAM cell presented for application in high speed, low power cache.

It is used to enhance the write ability of the SRAM cell using transmission gates and further modification is done in the write assist circuit to reduce the power consumption and delay. The proposed circuit gives better result. The 5T SRAM cell is proposed with fast performance and low power consumption.

1) Leakage Current Sensor and compensation circuit.

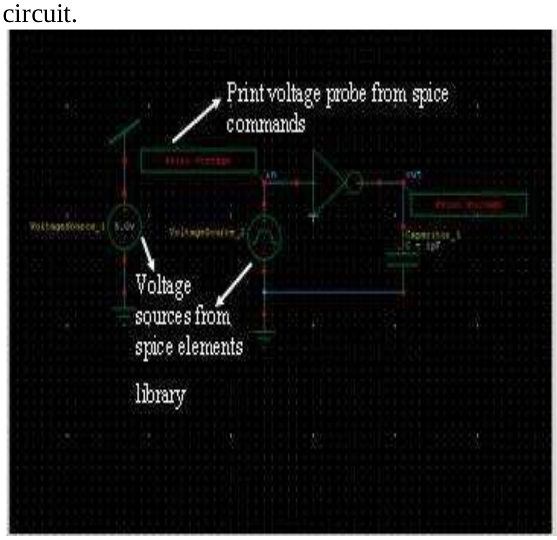

Fig 5 Schematics of leakage current sensor and compensation circuit.

Fig.5 Show the schematics of leakage current sensor and compensation circuit. A leakage current sensor consists of an SRAM cell model and a comparator. Since a larger leakage will result in low operating frequency, high power consumption, and even status flip in the SRAM cell. Comparator will notify a warning signal to activate the following compensation circuit. A Compensation circuit will speed up the read operation of SRAM if the leakage is detected and confirmed. SRAM cell model is used as a leakage monitor generating a voltage proportional to the leakage current, v_leakage, for comparator. If v_leakage is higher than v_ref, comparator will notify a warning signal to activate the following compensation circuit.

In this paper, we couple the node Q of 32 SRAM cells together and turn OFF all transistors to serve as the SRAM cell model. The reason is when the nodes Q of many SRAM cell are coupled together, the corresponding leakages of these cells are steered to the same node such that the common Q node voltage, v_leakage, will be pulled high almost proportionally. SRAM Operation An SRAM cell has three different states it can be in: standby where the circuit is idle, reading when the data has been requested and writing when updating the

. The SRAM to operate in read mode and write mode should have "readability" and "write stability" respectively. The three different states work as follows:

a) Standby: If the word line is not asserted, the access transistors M5 and M6 disconnect the cell from the bit lines. The two cross coupled inverters formed by M1 – M4 will continue to reinforce each other as long as they are connected to the supply.

b) Reading: Assume that the content of the memory is a 1, stored at Q. The read operation is done by using the sense amplifiers that pull the data and produce the output. The row decoders and column decoders are used to select the appropriate cell or cells from which the data is to be read and are given to the sense amplifiers through transmission gate.

c) Writing: The start of a write cycle begins by applying the value to be written to the bit lines. If we wish to write a 0, we would apply a 0 to the bit lines, i.e. setting BL bar to 1 and BL to 0. A 1 is written by inverting the values of the bit lines. WL is then asserted and the value that is to be stored is latched in. Note that the reason this works is that the bit line input-drivers are designed to be much stronger than the relatively weak transistors in the cell itself, so that they can easily override the previous state of the cross- coupled inverters.

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2) Read Delay Compensation

The details of the leakage compensation are as follows.

Step 1: v_leakage rises to indicate that the SRAM cell model is suffered from leakage currents.

2) Step 2: Once if v_leakage is higher than v_ref, comparator pulls low the warning signal.

Step 3: As soon as the warning drops, MP303 in compensation circuit is turned ON to pull-up BLb such that BL drops fast. In other words, a positive feedback is used to speed up the read access.

since the BLb will be predischarged at the beginning of each read operation, this compensate operation only operates, while data bit 0 is accessed. When reading data bit 1, it stays the same. Besides, the charging speed of the proposed compensation circuit is determined by the size of MP303 and MP304.

3) Row/Column Decoder

Row decoder is used to decode the address locations of memory. Row and Column decoder are necessary to access selected a cell. The simplest decoder is composed of NAND and NOR gates. A tree of two-input and three-input NAND gates and inverters using static CMOS logic possessing the lowest logical effort is used to build high fan-in gates in the decoders. In addition, those gates in row decoder in this design have two more inputs than those of the column decoder.

4) Build-In Self-Test

It is a mechanism that permits a machine to self test. The main purpose of BIST to reduces the complexity, and thereby decrease the cost .And reduces the complexity of the test/probe setup, by reducing the number of I/O signals that must be driven under tester control. A well-known basic memory testing methodology is the BIST circuit. The BIST circuit in this design is implemented based on March C-algorithm. March C-algorithm is a popular testing algorithm, which has medium fault coverage and complexity. It can detect stuck-at fault, transition fault, address-decoder fault, and coupling fault.

IV IMPLEMENTATION AND MEASUREMENT

To ensure the functionality and performance of the proposed SRAM cell, the dynamic noise margin (DNM) and SNM of the proposed SRAM cell, respectively, by simulations. The DNM is $\sim$0.3 V, which means that the state of the stored bit will not be interfered as long as the amplitude of the noise is lower than 0.3 V. the all-PT-corner simulation results of SRAM.

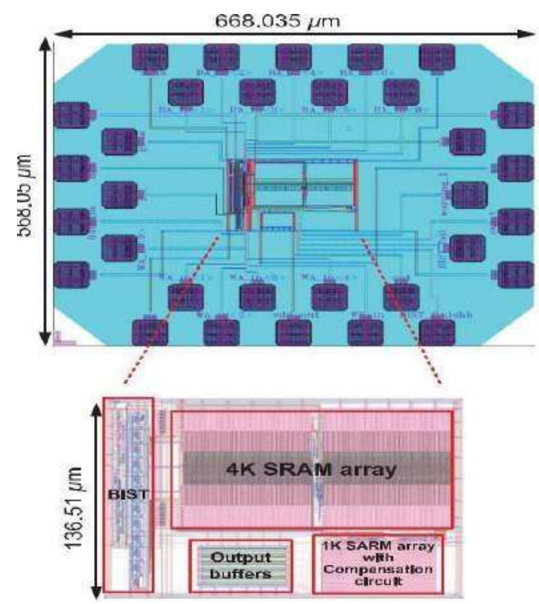

Fig.6 Layout of the proposed design SRAM

Layout of the proposed design SRAM in shown in fig 6. Two SRAM arrays are carried on the same die sharing common row decoder and column decoder. Notably, the 1-kb SRAM array with compensation only needs bit_addr, while the 4-kb SRAM array without compensation needs bit_addr.

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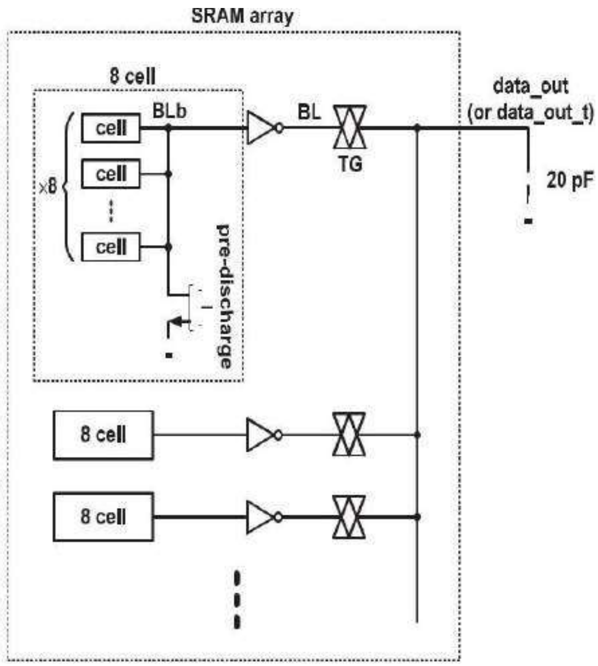

Fig.7 Schematic of the proposed SRAM array.

Fig.7 shows the schematic of the proposed SRAM array. Regarding the load of each node, the only one difference between 4- and 1-kb SRAM array is the output load of the transmission gate (TG). The amount of the TGs in a 4-kb array is four times more than that in a 1-kb array.

However, the output load of the SRAM arrays (about 20 pF, composed of pad, bonding wire, and probe) is much larger than the total parasitic capacitance of the transmission gates (about $2^9 \times 0.5$ fF in 4 kb and $2^7 \times 0.5$ fF in 1 kb) such that the total parasitic loads are negligible compared with the output load. Therefore, the output load of the transmission gate in 1- or 4-kb arrays is almost equal.

The leakage will slow down the entire read access, especially in the scenario of state 0 is to be read. Therefore, a compensation circuit consisting of two pMOS keepers, MP303 and MP304, speeds up the read operation such that the inverter and the following logic circuits can quickly pass the triode region to reduce power dissipation.

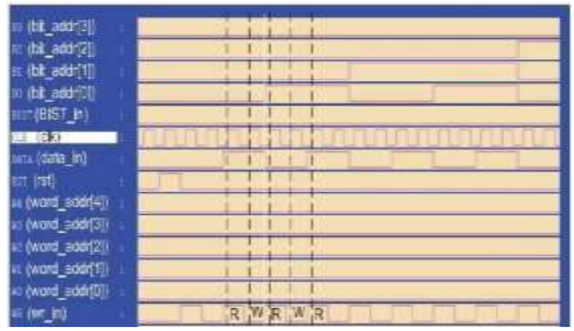

Fig.8 Measurement result of write/read operations

Fig.8 shows the write/read function test. The shown testing process of the write/read function test is (*w*0, *r* 0) then (*w*1, *r* 1). The starting address is 12’b000000000000 and up counts every four clock cycles. Notably, the voltage level of the output pin data_out is kept logic 1 during the write access.

The MATLAB turns to simulation and implement results Fig.9 describes when design with the MATLAB coding use to show the leakage current compensation.

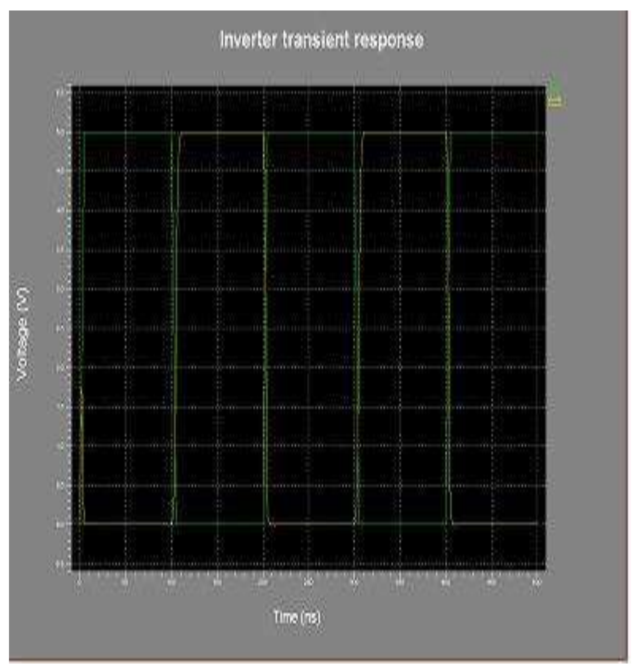

Fig.9 Waveform Analysis with MATLAB coding

To compare the proposed SRAM with prior works, a figure-of-merit (FOM) used in Table I is given

Table I performance Comparison

PARAMETERS	**VLSI'11**	**ISQED'12**	**TCAS-II'12**	**TCAS-I'14**	**PROPOSED**
NO OF TRANSISTER	8T	8T	9T	12T	5T
ENERGY/ ACCESS (pJ)	8.8	11.8	3.86	16	0.94811
DELAY (ns)	118.9	132	98.67	72	54.88

Comparsion of Existing and Proposed method graphs is shown in fig 10.

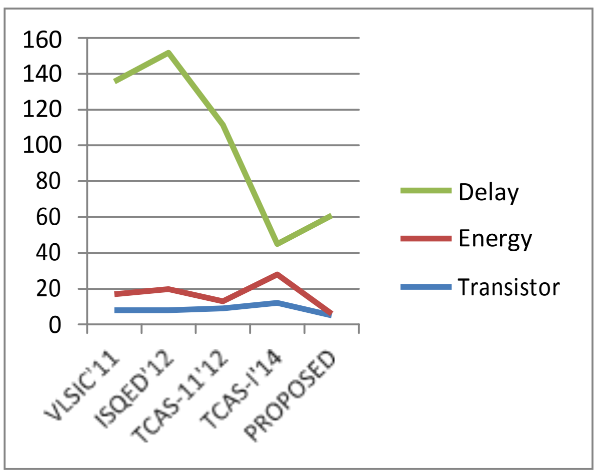

Fig 10 Comparison of Existing & Proposed Methods

V. CONCLUSION

The proposed SRAMs cell is implemented with transmission gate. A current mode sense amplifier which is proved to achieve low power and high speed is presented. Its sensing delay is independent of the capacitances. Its sensing delay and power consumption are almost independent of the bit- and data-line capacitances. In the proposed SRAM topology, additional circuitry has been added to a standard 5T-SRAM cell to improve the static noise margin (SNM) and the performance. At 0.6 V system voltage, the read delay is reduced 54.88% the proposed compensation design reduces 27.86% of the average power dissipation. The proposed Static Random-Access Memory is implemented using the TSMC 40-nm CMOS logic technology.It is reduces the power consumption and read delay.

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