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CLOCK PAIR SHARED FLIP-FLOP USING DOUBLE EDGE TRIGGERING TECHNIQUE FOR LOW POWER AND HIGH SPEED CLOCK DISTRIBUTION

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ABSTRACT- Logic signals the FF receivers retain VM compatibility with low-power CMOS logic in the remainder of the chip. This paper presents the first true CM CDN and a new CM pulsed D-type FF where the clock (CLK) input is a CM receiver and the data input (D), an active low enable ,and output (Q) are VM.A new paradigm for clock distribution that uses current, rather than voltage, to distribute a global clock signal with reduced power consumption. While current-mode (CM) signaling has been used in one-to-one signals, this is the first usage in a one-to-many clock distribution network. To accomplish this, a new high-performance current-mode pulsed flip-flop with enable (CMPFFE) using 45 nm CMOS technology. When the CMPFFE is combined with a CM transmitter, the first CM clock distribution network exhibits 62% lower average power compared to traditional voltage mode clocks. Transistor-based power-gating is implemented by placing sleep transistors in-line between the circuit and the power network or the ground network.

***Index Terms*—Clock distribution network, crosstalk, current-mode, flip-flop, low-power, power gating.**

I. INTRODUCTION

Recently, low-power design has become quite critical in synchronous application specific integrated circuits (ASICs) and system-on-chips (SOCs) because interconnect in scaled technologies is consuming an increasingly significant amount of power. Researchers have demonstrated that the major consumers of this power are global buses, clock distribution networks (CDNs), and synchronous signals in general. The CDN in the POWER4 microprocessor, for example, dissipates 70% of total chip power. In addition to power, interconnect delay poses a major obstacle to high-frequency operation. Technology scaling reduces transistor and local interconnect delay while increasing global interconnect delay. Moreover, conventional CDN structures are becoming increasingly difficult for multi-GHz ICs because skew, jitter, and variability

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are often proportional to large latencies. Prior to and in early CMOS technologies, current-mode (CM) logic was an attractive high-speed signaling scheme. CM logic, however, consumes significant static power to offer these high speeds. Because of this, standard CMOS voltage-mode (VM) signaling has been the de facto standard logic family for several decades. Low-swing and current-mode signaling, however, are highly attractive solutions to help address the interconnect power and variability problems.

Traditionally, the static power dominates dynamic power consumption in a CM signaling scheme. However, the static power is often significantly less than VM dynamic power and latency is significantly improved over VM in global CM interconnect. CM signaling schemes also offer higher reliability since are less susceptible to single-event transient upsets due to the absence of buffers with source/drain diffusion areas that can be hit by high-energy particles. Previous CM schemes have been used for commonly, offchip signals. Standard logic signals, however, have remained VM to benefit from the low static power of CMOS logic.

As transistor sizes scale down and levels of integration increase, leakage power has become a critical problem in modern low-power microprocessors. This is especially true for ultra-low-voltage (ULV) circuits, where high levels of leakage force designers to choose relatively high threshold voltages, which limits performance. In this thesis, an industry-standard technique known as power-gating is explored, whereby transistors are used to disconnect the power from idle portions of a chip. Present power-gating implementations from limitations including non-zero state leakage, which can aggregate to a large amount of wasted energy during long idle periods, and high energy overhead, which limits its use to long-term system-wide sleep modes. As this thesis will show however, by vastly increasing the effectiveness of power-gating through the use of emerging technologies, and by implementing aggressive hardware-oriented power-gating policies, leakage in microprocessors can be eliminated to a large extent. This allows the threshold voltage to be lowered, leading to ULV microprocessors with both low switching energy and high performance.

A. Literature review

The Literature [1] reviews a number of low swing on-chip interconnect schemes and presents a thorogh analysis of their effectiveness and limitations.The performance of each of the presented circuits is thoroughly examined using simulation on a benchmark interconnect circuit. The Literature [2] reviews the fourth generation power processor chip contains 170M transistors and includes 2 microprocessor cores.It is implemented in a 0.18/spl mu/m SOI technology, with 7 layers of Cu interconnect, and functions in systems at 1.1 GHz and dissipates 115W at 1.5V. The literature [3] reviews the characterization of on-chip interconnect is considered with particular attention to ultrasmall capacitance measurement and in-suit noise evaluation techniques. An approach to measuring femto-Farad level wiring capacitance is presented that is based on the concept of supplying and removing charge with active devices.The Literature [4] reviews the global wire delay becomes a major bottleneck in realizing high

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performance SOCs.Apart from the thecnological efforts being made to overcome the problem.It is necessary to develop new circuit design techniques. The Literature [5] reviews the high performance clock distribution has been a challenge for nearly three decades. This provides a thorough discussion of current issues in clock synthesis and conclude with insight into future research and design challenges for the community at large.

cope of this Paper

It is not practical to make each individual point-to-point segment of the CDN CM, but the clock signal should still benefit from the power and reliability of CM signaling. Instead, the power savings is maximized by creating a high-fanout physically or electrically symmetric distribution that feeds many CM flip-flop (FF) receivers. Logic signals the FF receivers retain VM compatibility with low-power CMOS logic in the remainder of the chip. This project, present the first true CM CDN and a new CM pulsed D-type FF where the clock (CLK) input is a CM receiver and the data input (D), an active low enable ,andoutput (Q) are VM.

II LOW POWER CLOCK DISTRIBUTION USING CURRENT PULSED CLOCKED FF WITH ENABLE

Low-swing and current-mode signaling, however, are highly attractive solutions to help address the interconnect power and variability problems. Traditionally, the static power dominates dynamic power consumption in a CM signaling scheme. However, the static power is often significantly less than VM dynamic power and latency is significantly improved over VM in global CM interconnect. CM signaling schemes also offer higher reliability since this is less susceptible to single-event transient upsets due to the absence of buffers with source/drain diffusion areas that can be hit by high-energy particles. Previous CM schemes have been used for commonly, offchip signals. Standard logic signals, however, have remained VM to benefit from the low static power of CMOS logic.

In this scheme, it is not practical to make each individual point-to-point segment of the CDN CM, but the clock signal should still benefit from the power and reliability of CM signaling. Instead, the power savings is maximized by creating a high-fanout physically or electrically symmetric distribution that feeds many CM flip-flop (FF) receivers. Logic signals on the FF receivers retain VM compatibility with low-power CMOS logic in the remainder of the chip. In a CM signaling scheme, a transmitter (Tx) utilizes a VM input signal to transmit a current with minimal voltage swing into an interconnect (transmission line), while a receiver (Rx) converts current-to-voltage providing a full swing output voltage. The representative CM scheme uses a CMOS inverter as the Tx while the Rx is based on a transimpedance amplifier.

A. Previous CM Signaling scheme

In a CM signaling scheme, a transmitter (Tx) utilizes a VM input signal to transmit a current with minimal voltage swing into an interconnect (transmission line), while a receiver (Rx) converts current-to-voltage providing a full swing output voltage. The representative CM

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scheme uses a CMOS inverter as the Tx while the Rx is based on a transimpedance amplifier. This scheme provides delay improvement over VM schemes, but the Rx voltage swings would cause a large CDN skew. Other researchers have used a dynamic over-driving Tx with a strong and weak driver alongside a low-gain inverter amplifier Rx and a controlled current source that addresses the previous problem. However, this scheme results in rise- and fall-time mismatch at the output which can be problematic in CDNs. Variation-tolerant CMsignaling schemes have used a CM Tx with corner-aware bias circuitry.

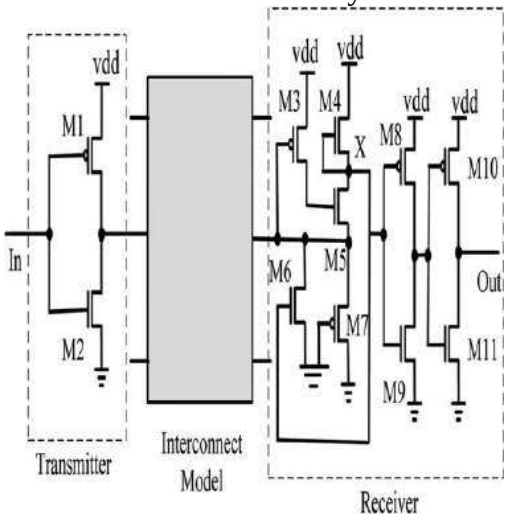

Figure 1.Previous CM schemes used an expensive transimpedance amp Rx which could result in significant skew due to shift if applied to CDNs

The variation tolerant CM scheme including Rx and Tx circuits is shown in the Figure 1. In this scheme, the inverter amplifier Rx circuit provides low-impedance to ground and holds the terminal point at the switching threshold. However, this comes at the expense of large static and dynamic power when compared to the other CM techniques and makes it unattractive compared to existing VM signaling.

It is possible to use a local or global reference voltage generatorfor the input gate voltage of M4. Using a global reference can increase the robustness by reducing transistor mismatch between FFs. Hence, it used a global reference voltage generator that distributed across the whole chip, when integrate the CMPFFE with the CM CDN. This also saves two transistors per FF and reduces static power with a negligible performance penalty. Unlike corner-aware reference voltage. In addition, CM signaling eliminates the requirement of CDN buffers, which reduces significant active area and makes easier global reference routing.

However, driving the lowest level of a CDN with afull-swing voltage results in large dynamic power in addition to significant buffer area to drive the clock pin capacitances. This CM scheme is highly integrated into the FFs that directly receive the CM signal to reduce overall power consumption and silicon area.The CMPFFE is similar to the previously published CMPFF, but uses an active-low enable signal. The CMPFFE uses an input current-comparator (CC) stage, a register stage,and a static storage cell.

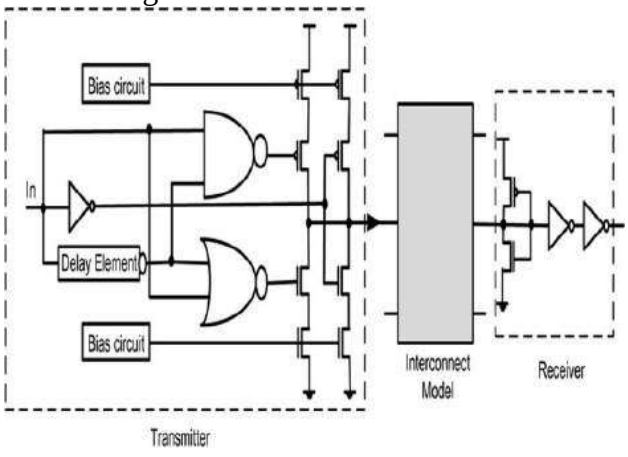

Figure. 2 Expensive variation tolerant CM signaling scheme consumes large static and dynamic power when compared to the other CM techniques.

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The feedback connection from the generated voltage pulsewith M6 quickly pulls down the current comparator node B which facilitates generating a small voltage pulse and resultsin fewer transistors in the register stage. In addition, it properly size the X2 inverter so that it can efficiently drive the clock capacitance of register stage without affecting circuit performance.This comes at the expense oflarge static and dynamic power when compared to the otherCM techniques and makes it unattractive compared to existing VM signaling.This scheme results in rise-andfall-time mismatch at the output which can be problematic in CDNs.

III. PROPOSED SYSTEM

A.Current-Mode Transmitter and Distribution

In order to integrate the CMPFFE, a Tx provides a pushpullcurrent into the clock network and distributes the required amount of current to each CMPFFE.The Tx receives a traditional voltage CLK from a PLL/clock divider at the root of the H-tree network and supplies a pulsed current to the interconnect which is held at a near constant voltage. The clock distribution is a symmetric H-tree with equal impedances in each branch so that current is distributed equally to each CMPFFE leaf node. The NAND gate uses the CLK signal and a delayed inverted CLK signal, clkb, as inputs to generate a small negative pulse to briefly turn on M1. Hence, the PMOS transistor briefly sources charge from the supply while the NMOS is off. Similarly, the NOR gate utilizes the negative edge of the CLK and clkb signals to briefly turn on M2. Hence, the NMOS transistor briefly sinks current while the M1 is off.

B. Double Edge Triggering

Transistor-based power-gating is implemented by placing sleep transistors in-line between the circuit and the power network (headers) or the ground network (footers). Footers are generally more area-efficient as the high n-type mobility means less of them are needed. That being said, most commerical designs implement headers due to easier design and analysis,

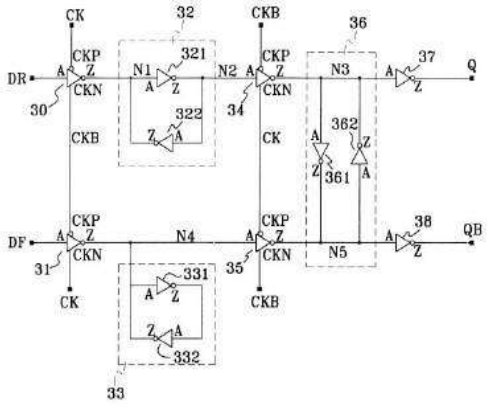

Figure 3 Circuit of the proposed clocked pair shared flip-flop using double edge trigerring technique

especially when multiple power domains or an external switchable voltage regulator is use. First, the headers themselves leak which means leakage is reduced, but not eliminated.Second, when the headers are on, the current owing though them creates a voltage drop on the power network that lowers the performance of the power-gated circuit . This performance drop is especially severe with ULV processors, where delay is exponentially dependent on supply voltage; in this region, a small variation in voltage leads to a very large drop in

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performance.The controlling factor of the trade-0_ between delay increase and 0_-state leakage reduction is the width of the headers. A common industry practice is to size the headers such that the worst-case supply voltage drop is less than 10%, but this results in a large area overhead, and generally the sleep-mode leakage reduction is only around 90%. During long idle periods, this remaining leakage can lead to significant amounts of wasted energy. The ultra-low power Phoenix processor took the opposite route and used a small amount of footers with non- minimal channel lengths. This resulted in picowatt-range 0_-state power, but the large supply voltage drop limited the clock frequency to 106 kHz. This trade-0, and the desire to achieve a large

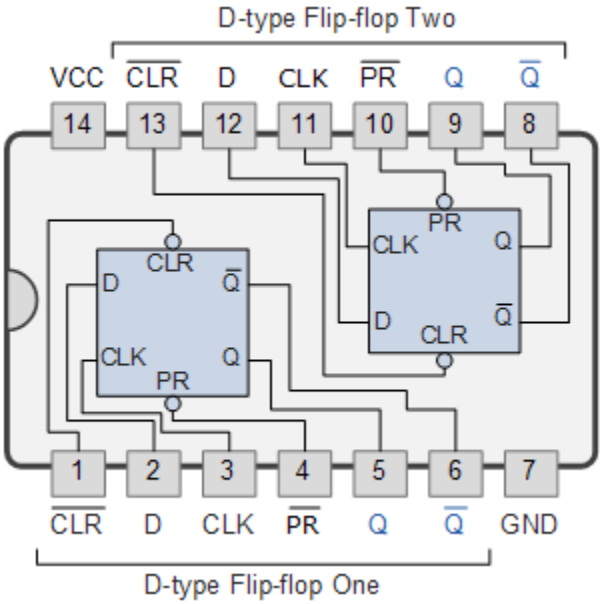

Figure 4 Double Edge Triggering Flip Flop

reduction in 0_-state leakage without impacting performance motivates one of the examinations in this thesis, where an emerging technology, the CMOS-Compatible NEMS switch, is used as a power-gating structure.

C. SIMULATED RESULT

The clock distribution network distributes the clock signal from a common point to all the elements that need it. Since this function is vital to synchronous system, much attention has been given to the characteristics of these clock signal and the electrical networks used in their distribution. The performance of the FFs was evaluated using post-layout SPICE simulation at clock frequencies from 2–5 GHz with less than 10 psslew and a 1 V supply voltage.Figure.3 shows theSchematic of the proposed clocked pair shared flip-flop using power gating technique for low power and high speed clock distribution network. The power considers input data at 100% activity and 4 minimum size inverter load. In order to validate the functionality of the CM Tx and the proposed CMPFFE in a CDN, implemented a symmetric H-tree network spanning 1.2 mm 1.2 mm. Figure 5 Layout Design of the proposed clocked pair shared flip-flop using power gating technique for low power and high speed clock distribution network.

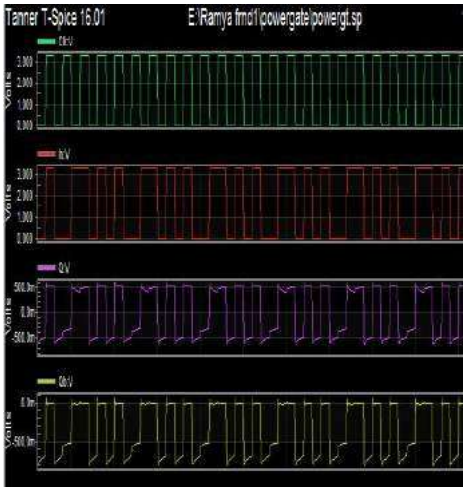

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Figure 5 Output of the proposed clocked pair shared flip-flop using double edge triggering technique

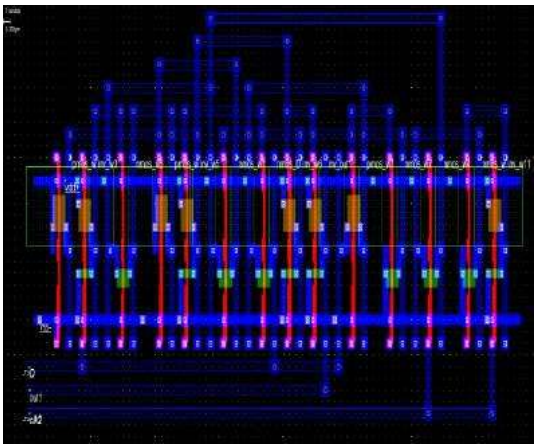
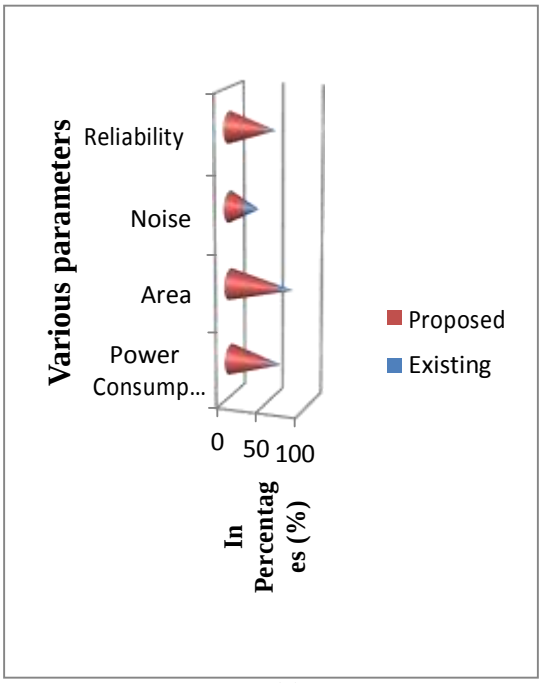
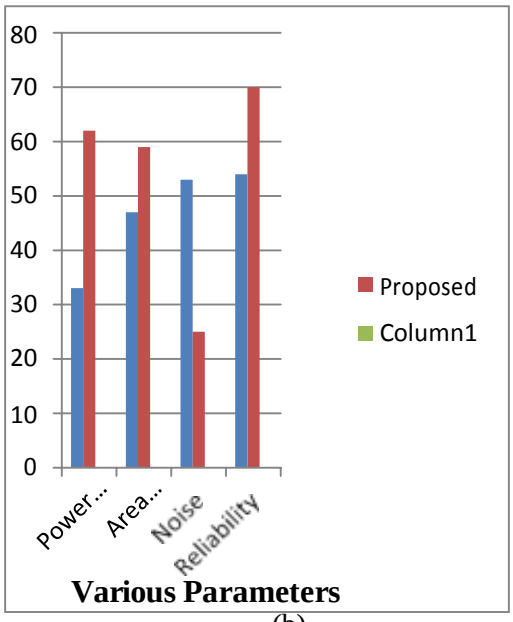


Figure 6 Layout Design of the proposed clocked pair shared flip-flop using double edge triggering technique



(a)



(b)

Figure.7 (a) and (b)**Graph comparision of Exisiting and Proposed method**

IV. CONCLUSION AND FUTURE ENHANCEMENT

The proposed Current Mode Pulsed Flip-Flop with Enable(CMPFFE) is 87% faster, requires similar silicon area and consumes only 7% more power compared to a traditional PFF at 5 GHz. Better yet, the CMPFFE enables a 24% to 62% power reduction on average when used in a CM CDN compared to conventional VM CDNs. The CMPFFE also eliminates the need for complex CM Rx circuitry and/or local VM buffers to drive highly capacitive clock sinks as in previously proposed CM signaling schemes.

The CM Clock distribution Network exhibits lower average power when compared to voltage mode clock. In future, further power reduction is going to be achieved by using power gatting technique and reducing the number of transistors and hence further layout size can be reduced.

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