COMPARISON OF LIFT CONTROLLER DESIGN BASED ON VERILOG

J.Megan David M.E., M.Suresh M.E.,

Assistant Professor, EEE Department, DMICE

Abstract: **The fast growth in the semiconductor industry over the past twenty years has put Very Large Scale Integration in high demand all over the world. The basics of digital logic theory and techniques can be easily understood by the design based on VLSI technology. These are the core fundamentals of the fast, high-speed complex digital circuits. As time goes by the technology is gradually improving. So obviously, the designs must be made simpler for getting its benefits. To do that, a Three-Lift Controller is modelled. In the proposed work, a VERILOG RTL code is developed to control the lift movement based on the request it will receive. By that a finite state machine is developed to know from which state the controller is changing based on the requests coming from the end user. This design is based on the synchronous input which should be operating with a fixed sort of frequency. At the end, the RTL is verified and implemented in XILINX ISE. In this paper, the real-time three-lift controller will be modelled with Verilog HDL code using Finite-State machine (FSM) model to achieve the logic in an optimized way.**

Keywords: FSM, Controller, Elevator control.

I. INTRODUCTION

An elevator is defined as a device designed as a convenience appliance that has turned to become an unavoidable feature of modern day urban life. An elevator is a machine that carries people or goods up and down to various levels in a building". While a standalone elevator is a simple electro-mechanical device, an elevator system may consist of multiple standalone elevator units whose operations are controlled by a master controller. Such controllers are designed to work with maximum efficiency in terms of operation as well as resource utilization. This paper details the design of an elevator controller using VERILOG HDL.

The Elevators/Lifts are used in multi storey buildings as a means of transport between various floors. Elevator is a device designed to be a convenience appliance which has evolved to become an indispensable feature of modern day in human life normally. Currently, the lifts are controlled by Microprocessor based systems, which are relatively costlier. It is proposed to design a compact dedicated controller of low cost. The Elevator Controller is a device used to control the motion of the lift and to indicate the direction of movement, and the present floor level, etc. The device controls the lift motion by accepting the floor level as input and generate control signals (for control the lift motion) as output.

We developed a VERILOG code for 3-storey elevator control system to make the elevator to move up and down. The designing and simulation of the Elevator controller unit can be performed using VERILOG HDL. Also, the Timings of different signals can be verified. VERILOG is a hardware description language used in electronic design automation to describe digital and mixed-signal systems such as field-programmable gate arrays and integrated circuits.

The key advantage of VERILOG when used for designing a system is that it allows the behaviour of the required system to be described (modelled) and verified (simulated) finally synthesis tools translate the raw design into a real hardware. VERILOG project is multipurpose one. Being created once, the block can be used in many projects. However, many formational and functional block parameters can be tuned such as capacity parameters, memory size, element base, block composition and interconnection structure.

II. PRINCIPLE OF ELEVATOR CONTROLLER

Elevator controller is a basic system which consists of elevators serving 3 floors. The elevator car has a few control buttons (up / down) for moving the elevator up and down. The car also has call buttons to call for service of the elevator system. The Principles used for the design of the elevator controller are as follows:

- ✓ The floors are defined as first floor and second etc. A floor call is serviced using the elevator.

- ✓ Upon arrival at a floor, the doors open immediately.
- ✓ Doors remain open before closure.
- ✓ If an obstruction is detected when door is about to close, it remains open
- ✓ Each elevator car is treated as a sub-system controlled by the controller.
- ✓ Elevator Up / Down buttons are connected to elevator units.
- ✓ Each door unit is treated as a subsystem controlled by the respective elevator car.
- ✓ Floor call buttons are connected to the elevator controller.

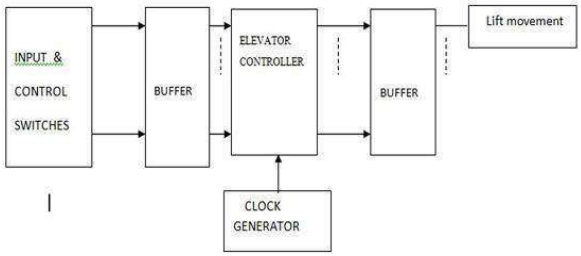

Fig 1. Block Diagram of Elevator Control Unit

A. STATE FLOW OF CONTROLLER:

The entire elevator controller system has been considered as a collection of smaller sub-systems i.e., door units, elevator units and the master controller. The following section describe these subsystems.

B. ELEVATOR UNITS:

The elevator units are controlled by the master controller with the help of a set of elevator commands. The status of each of the elevator units is given to the master controller as an input. The Table below shows the design commands and the corresponding state transitions.

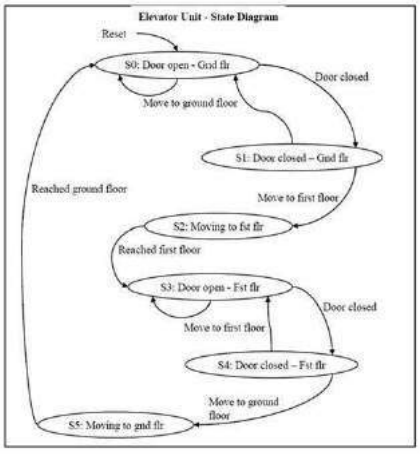

Fig 2. Model Flow Diagram for the Elevator Unit

III. RESULTS AND CONCLUSIONS

A. SIMULATION RESULTS:

In this paper, the proposed design uses Xilinx-ISE tool for logical verification, and also synthesizing it on Xilinx-ISE tool using target technology and performing P and R operation for system verification. Figure 3 shows the simulation result of the designed elevator controller and Figure 4 & 5 shows the RTL schematic of the design.

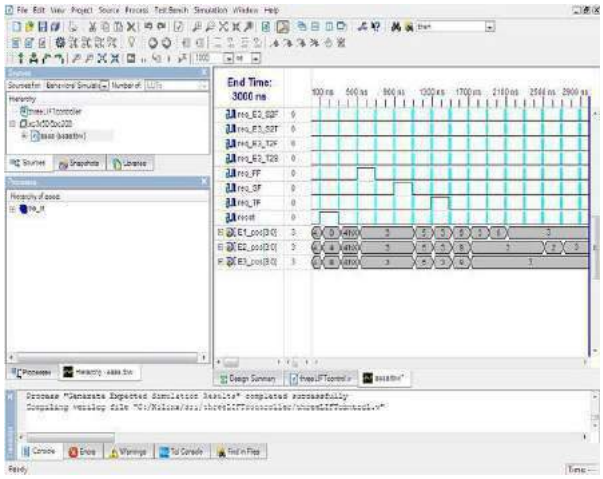

Fig 3. Simulation Results

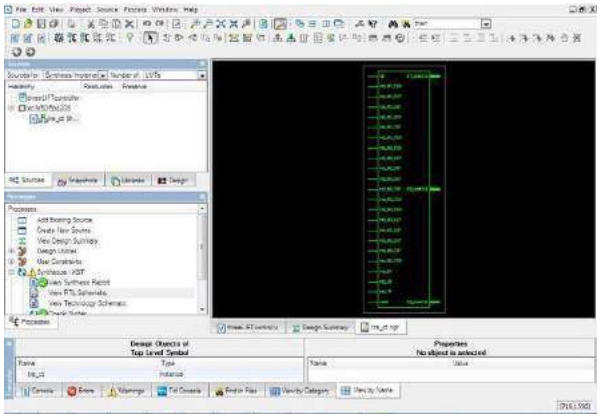

Fig 4. RTL Schematic

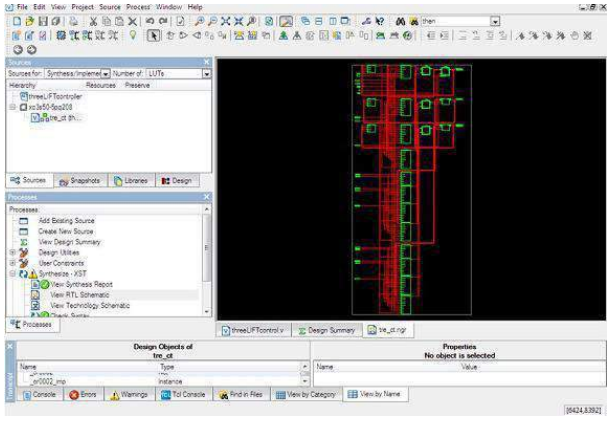

Fig 5. RTL Floor Plan

B. CONCLUSION:

The device utilization summary is shown in Table 1. From the device utilization summary, it can be seen that the resources that consumed for developing this system is very less.

TABLE I. DEVICE UTILIZATION SUMMARY (ESTIMATED VALUES)

Logic Utilization	Used	Available	Utilization
Number of Slices	20	768	2%
Number of Slice Flip Flops	24	1552	1%
Number of 4 Input LUTs	31	1552	2%
Number of Bonded IOBs	32	124	25%
Number of GCLKs	1	8	12%

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