DDFS based on Modified Taylor Series Approximation with Piecewise Linearization

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Abstract — **The ultimate choice for signal generation is direct digital frequency synthesis (DDFS) which is gaining more popularity among modern communication systems. DDFS is capable of generating a digitally controllable and digitally tunable signal frequency. The existing conventional DDFS architectures requires large read only memory (ROM) and more hardware overhead, which ultimately increases the power consumption of the system. This paper proposes a DDFS architecture with smaller read only memory and minimum hardware overhead. It is based on the modification of the Taylor series approximation based on Piecewise Linearization approach. The proposed method has the advantage of high spectral purity, low power consumption and high speed. The proposed DDFS architecture is able to achieve a spectral purity of about 170 dBc.**

Keywords— direct digital frequency synthesis; read only memory; Taylor series; Piecewise Linearization; spectral purity; DDFS architecture

I. INTRODUCTION

Generating a digitally controllable and tunable waveform is of a great concern, because in many areas, the ability to generate waveform with high spectral purity, minimum noise level and low spurious signal content is needed. Also, the communication systems demand maximum frequency tuning resolution with minimum quantization error. The cost, chip area, power consumption and memory size are the deciding factors for preferring one design over the other.

The method of generating desired waveform from a fixed frequency reference signal is called frequency synthesizers. There are various possibilities of this method such as analog frequency synthesizers or digital frequency synthesizers. But the most convenient method which fits the constrain is the direct digital frequency synthesis. A Direct Digital Frequency Synthesizer (DDFS) produces an analog waveform by generating a time-varying signal in digital form and then performing a digital-to-analog (D/A) conversion. The most common analog waveform generated by this approach is the sine waveform, since according to Fourier synthesis, any waveform can be decomposed into sum of pure sinusoids. This digital approach of generating a sinusoidal signal has an advantage of fast switching between output frequencies, fine frequency resolution, fast settling time, low phase noise and spurious noise and operation over a broad spectrum of frequencies.

ROM based DDFS [3] uses Look-up Table (LUT) of sampled sine values of a complete cycle and accessing it depending on the output frequency required. But this method has several drawbacks including large chip area and high power consumption. Common methods employed to reduce the size of the ROM are quarter wave symmetry [9]. Algorithmic methods such as CORDIC can be used as a replacement for the ROM by calculating the phase to amplitude conversion in digital circuitry [6]. However, the additional digital circuits increase the chip area and power consumption [10].

To overcome the problems associated with look-up table and algorithm based systems, the sine and cosine functions are approximated using extended Taylor series approximation [14]. However, computation of the expansion polynomial requires considerable multiplier hardware which increases the complexity of the system. To reduce the complexity, a piecewise linearization method of approximation is proposed. The spectral purity of the system is greatly improved in addition to the reduction in hardware. However, the reduction of multiplication is at the cost of extra memory to store the polynomial coefficients, as well as the function values of the expansion points. Thus, the system has less hardware, high operating speed and memory is also reduced, thus reducing the power consumption of the system.

II. PROPOSED DDFS ALGORITHM

The proposed DDFS design provides minimizing the size of the ROM lookup table by using an approximation algorithm with a judicious choice of polynomial [8]. The primary objective for using such an approach is that precision can be achieved with relatively less hardware overhead when compared to other techniques of sine wave generation. The resulting low-power architecture meets the specifications of low power communication standards such as Bluetooth [2].

The performance of the system depends on the size of the DDFS architecture.

A. *Trigonometric and Extended Taylor Series approximation using Piecewise Linearization Algorithm*

1) *Sine (γ_s) and Cosine (γ_c) Accumulator*

In the Taylor series expansion, the Sine and Cosine functions can be implemented at a point γ (constant) given by neglecting higher order terms,

$$\sin(\theta) \sim \sin(\gamma) + (\theta - \gamma)*\cos(\gamma) \quad (1)$$
$$\cos(\theta) \sim \cos(\gamma) - (\theta - \gamma) * \sin(\gamma) \quad (2)$$

Another form of Taylor series expansion for sine and cosine function at a point γ is given by neglecting higher order terms,

$$\sin(\gamma) \approx \gamma \quad (3)$$
$$\cos(\gamma) \approx 1 - (\gamma^2/2!) \quad (4)$$

By applying Equation (3) and (4) in Equation (1),

$$\sin(\theta) \approx \left(1 - (\gamma^2/2!)\right) * \theta \quad (5)$$
$$\gamma_s = \sqrt{\left(2 * \left(1 - (\sin(\theta)/\theta)\right)\right)} \quad (6)$$

Similarly, by applying Equation (3) and (4) in Equation (2),

$$\cos(\theta) \approx \left(1 + (\gamma * \gamma/2)\right) - (\theta * \gamma) \quad (7)$$
$$\gamma_c^2 - 2(\theta * \gamma_c) - 2(\cos(\theta) - 1) = 0 \quad (8)$$

where, θ ranges from 0º to 45º. The minimum of the two roots from equation (8) is used for the computation.

2) *Linear Approximation*

To reduce the complexity of sine and cosine accumulator, the equation approximated by means of a linear equation which can be constructed easily using an accumulator and a comparator.

The linear equation for sine accumulator is given by,

$$\gamma_s = (\gamma_{s,max} / \gamma_{s,step}) * \theta \quad \text{(for } \theta \text{ varies from 0 to } \pi/4) \quad (9)$$

Where, $\gamma_{s,max} = \gamma_s$ (for $\theta = \pi/4$)
$\gamma_{s,step} = \gamma_{s,max} / (\pi/4 * 2^N)$

Similarly, the linear equation for cosine accumulator is given by,

$$\gamma_c = (\gamma_{c,max} / \gamma_{c,step}) * \theta \quad \text{(for } \theta \text{ varies from 0 to } \pi/4) \quad (10)$$

Where, $\gamma_{c,max} = \gamma_s$ (for $\theta = \pi/4$)
$\gamma_{c,step} = \gamma_{c,max} / (\pi/4 * 2^N)$

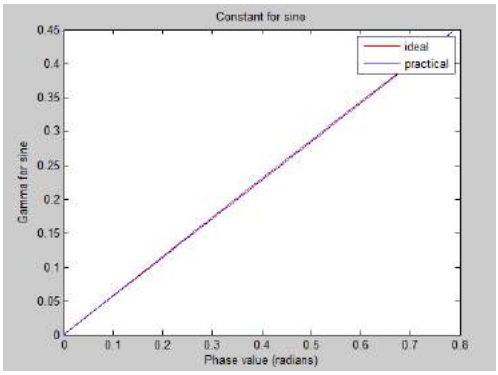

Fig. 1. Deviation in theoretical γ values and linear increment of γ values for sine

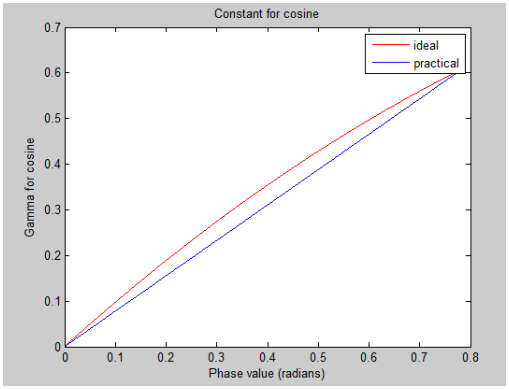

Fig. 2. Deviation in theoretical γ values and linear increment of γ values for cosine

Fig. 1 shows the comparison between theoretical and the linear increment values of γ_s. It is inferred from the graph that the linear increment γ_s values are in line with the theoretical γ_s values. But, the variation between theoretical γ_c and linear increment γ_c is slightly larger due to the strong dependency of cosine function with γ. This can be observed from Fig. 2.

3) *Piecewise Linearization*

The slight deviation between theoretical γ_c and linear increment γ_c is reduced by using piecewise linearization. Piecewise linearization of theoretical γ_c is done by dividing the region into several subintervals. In turns, each subinterval carries out its own linear approximation. The accuracy of the output signal depends on the degree of the reconstructing polynomial, the number of subsections, the word length of the truncated phase accumulator output, as well as the word length of the DDFS system output. However, this leads to an increase in the spectral purity of the generated signal, but with some hardware overhead. The purity of the signal varies in direct proportion to the number of linear segments. Fig. 3 shows piecewise linearization using four linear segments. It is observed that the spectral purity of the signal gets saturated to almost constant beyond four linear segments and hence four segment based piecewise linear approximation is proposed.

Let, points = 4 and i = 1,2,3,4

The piecewise linear equation is given by,

$$\gamma_{c,i} = ((\gamma_{end,i} - \gamma_{start,i}) / \gamma_{step,i}) * \theta \quad (11)$$

(for θ varies from 0 to π/4)

Where, $\gamma_{max} = \gamma_c$ (for θ = π/4)

$\gamma_{start,i} = (\gamma_{max} * 2^N) * ((i-1) / points)$

$\gamma_{step,i} = (\gamma_{max} * 2^N) / points$

$\gamma_{end,i} = (\gamma_{max} * 2^N) * (i / points)$

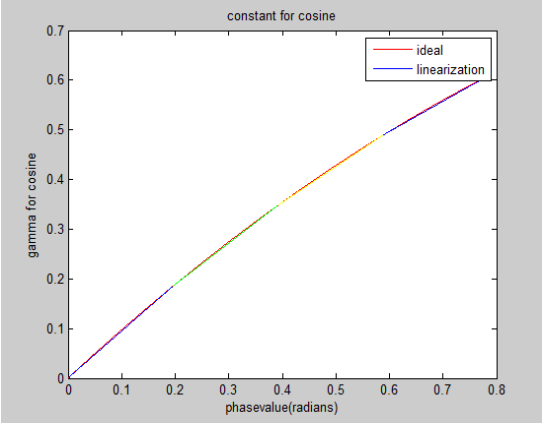

Fig. 3. Piecewise linearization of theoretical γ_c values with four uniform segments

III. PROPOSED DDFS ARCHITECTURE

Fig. 4 shows the block diagram of the proposed DDFS architecture. It consists of phase generator, quadrant selector, sine/cosine generator, digital multiplexers and a DAC in the output stage. The phase generator (PG) of the proposed DDFS receives an input as a frequency control word (FCW) from the system in which the proposed DDFS is integrated. The phase generator output is then fed to quadrant selector which selects the phase corresponding to the quadrant requirement. The output of the quadrant selector is fed to sine/cosine generator and any one of these output is selected and given to the input of the DAC. The multiplexer in the output stage selects the output of the generators either from sine generator or cosine generator to complete a full cycle of sinusoidal as discussed. The full cycle is generated by exploiting the symmetry of sine wave with respect to zero crossings over one full period.

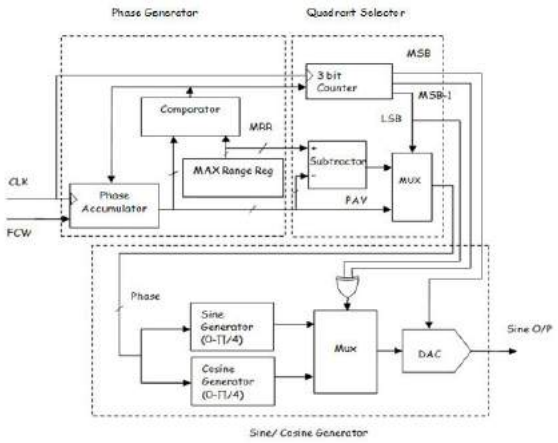

Fig. 4. Block Diagram of Proposed DDFS

A. *γ Accumulator sine and cosine based on piecewise linearization approach*

Fig. 5 shows the block diagram of the γ_s accumulator employed for generating γs values. It consists of an adder, latch, comparator, subtractor and a multiplexer. Also the module comprises of two registers, one register to store the γ value (γ_S value corresponding to $(\pi/4 * 2^N)$th clock cycle) and another register to store the γ step value (linear incremental step size of the γ) which is a product of frequency control word (FCW) and $\gamma_{max}/ (\pi/4 * 2^N)$.

For each clock input, the adder with the latch generates an accumulated γ value with the step size of$(\gamma_{max}/ (\pi/4 *2N))*FCW$. This accumulated γ value is fed to a comparator and a subtractor.

The comparator compares accumulated γ value with the γ_{max} value for every instance of clock. When the accumulated γ value reaches to γmax, the latch is cleared to zero and γ accumulation is started from initial value.

The subtractor subtracts accumulated γ value with the γ_{max} value for every instance of clock. The subtracted value of the γ accumulator is fed to multiplexer and the accumulated γ value is also given to the multiplexer. One of the inputs of the multiplexer is selected by the LSB of the counter in quadrant selector and given to sine/cosine generator.

Thus, γ accumulator is employed to generate γ_s values between 0 to π/4. Similar hardware architecture is used to generate γ_c values. Fig.6 shows the block diagram of γ_c accumulator. The primary difference between the architectures employed to generate γ_s and γ_c values lies in the γ_{max} register content. The appropriate values to be stored in the γ_{max} registers are determined from the above equations.

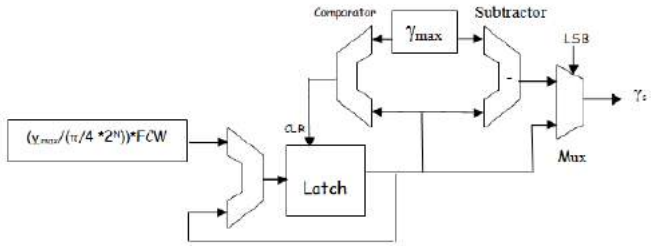

Fig. 5. Block Diagram of sine γ Accumulator

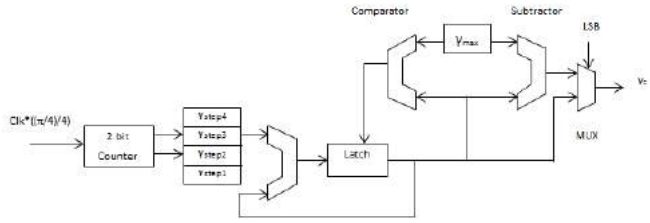

Fig. 6. Block Diagram of cosine γ Accumulator

IV. RESULTS AND DISCUSSIONS

A. *DDFS using LUT Based γ Values*

The computed γ values for sine ranging from 0.0003 to 0.4465 and cosine functions ranging from 0.0005 to 0.6091 for 12 bit resolution are stored in a LUT. For each increment of phase accumulator output, the corresponding γ values can be accessed from the ROM for computation. The performance of the DDFS using the LUT based γ values is nearly 230 dBc. Fig. 7 shows the spectrum obtained using these values. However, storing all γs and γc values in a lookup table greatly increases the hardware overhead and power consumption.

B. *DDFS using γ Accumulator*

Instead of using look up table for storing γ values, combinational circuits like adder and multiplier are used for the computation of γ values thereby reducing the computational time. Fig.5 shows the architecture of γ accumulator. A simple combinational circuitry can automatically generate the γ values if one knows the range of γ values that is the maximum and minimum values of γ, and the linear equation. Thus, using the linear increment γ values, the ROM size is drastically reduced.

γs is varied from 0 to γmax i.e., 0.4465 in steps of γ max/($\pi/4*2^N$). Similarly γc is varied from 0 to γmax i.e., 0.6091 in steps of γ max/($\pi/4*2^N$).Fig. 8 shows the spectrum for DDFS using γ accumulator. As it is seen from the graph, the SFDR performance of the DDFS using γs and γc accumulator over the range 0 - π/4 is about 135.6 dBc as compared to LUT γ values set of 230 dBc.

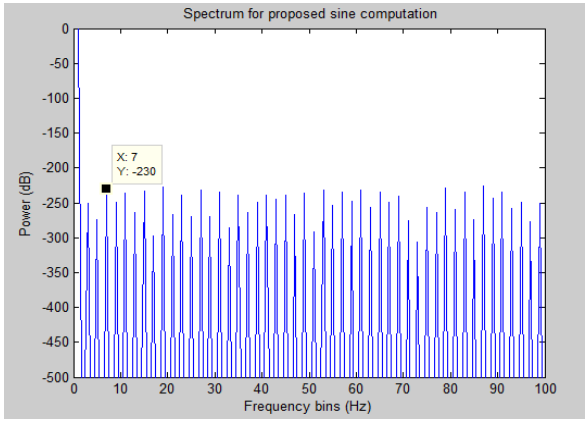

Fig. 7. Spectrum of the proposed DDFS using LUT for γ values

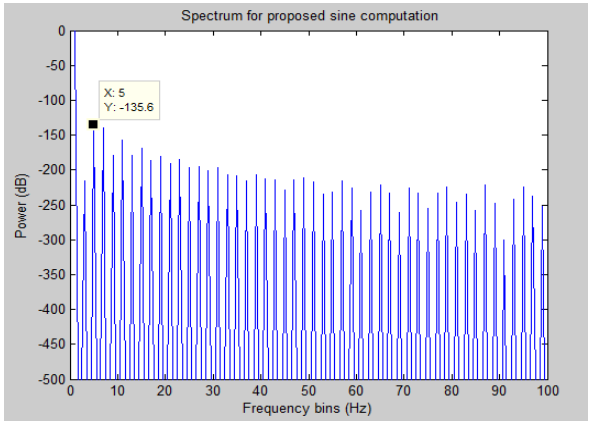

Fig.8. Spectrum of the proposed DDFS using γ accumulator

Fig. 9 shows the spectrum obtained using piecewise linearization with four linear segments. It is clear that the spectral purity of the signal is increased towards the theoretical γ value of 230 dBc. The SFDR value obtained with four uniform segments is about 169.4 dBc. The proposed method is compared with previous DDFS techniques as shown in Table I. The SFDR performance with various linear segments is shown in Table II.

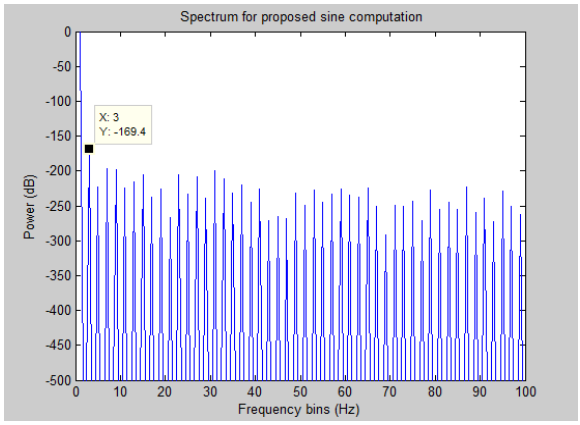

Fig. 9. Spectrum of the proposed DDFS using piecewise linearization with four uniform segments

TABLE I. Comparison with existing DDFS techniques

Ref.	Bit resolution	SFDR (dBc)	SNR (dBc)	Hardware Overhead / Comments
[2]	16	84.4	90.2	Multiplier Less, Pipelined Data Path
[6]	16	90.3	92	Polynomial Interpolation Methods
[14]	14	90	75	Two Segment Fourth Order Parabolic Approximation Technique
[15]	20	138	122	Two squares, four general multipliers and three 24-bit adders.
Proposed work	12	169.4	69	Modified Taylor series approximation and piecewise linearization

TABLE II. SFDR performance of the proposed method

No. of uniform Segments	SFDR (dBc)
3	168.4
4	169.4
5	170.1
6	170.3
7	170.7
8	170.8
9	170.9
20	171.3

V. CONCLUSION

In this paper, a novel low complexity DDFS architecture using modified Taylor Series approximation based on piecewise linearization has been proposed. It can be noted that the measured SFDR is 169.4dBc using piecewise linearization (four linear segments) with only 12 bit resolution, as compared to SFDR of 90.3 dBc with 16- bit resolution attainable with Polynomial Interpolation methods. Also, the piecewise linearization maximizes the SFDR for a given number of uniform segmentation. Since, linear increment of γ is used, the requirement of ROM has been reduced to minimal, thus reducing the hardware requirement.

ACKNOWLEDGMENT

The authors would like to express their deepest gratitude to K. Hariharan, Department of Electronics and Communication Engineering, for his continuous guidance, stupendous help, encouragement throughout this research.

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