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Monograph On Field Effect Transistors

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JFETs- Drain and Transfer Characteristics - Current Equations - Pinch off Voltage and its significance - MOSFET - Characteristics - Threshold Voltage - Channel length modulation, D-MOSFET - E - MOSFET - Current Equation - Equivalent circuit model and its parameters, FINFET, DUAL GATE MOSFET.

FIELD EFFECT TRANSISTOR (FET)

* 3 terminal semiconductor device
* Voltage controlled device

BASIC DIFFERENCE BETWEEN BJT AND FET:

* BJT→ bipolar device; FET → unipolar device
* Current through FET is controlled by voltage whereas current through BJT is controlled by current.

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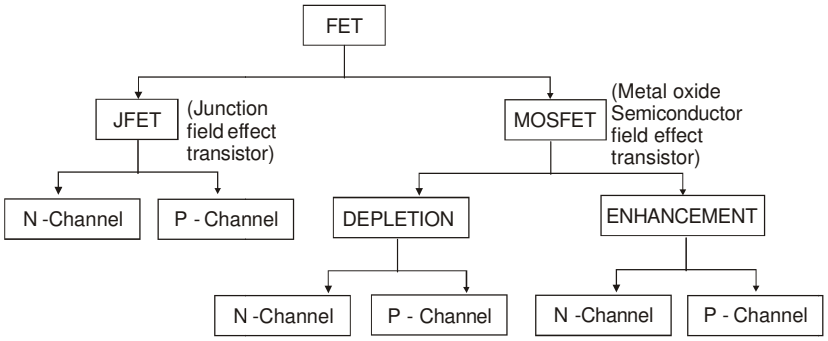
CLASSIFICATION OF FET:



FEATURES OF FET:

* Operation of FET depends upon flow of majority carriers only.
* High input impedance
* Less noisy than BJT
* Simple to fabricate
* Occupies less space in IC's

x

3.1.4 JUNCTION FIELD EFFECT TRANSISTOR (JFET):

(May /June 2011 - 16 Marks, Nov/ Dec - 2010 - 16 Marks, May /June 2012 - 16 Marks)

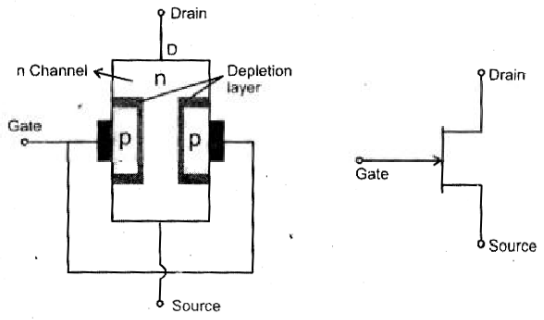


Fig 3.1 (a) n Channel JFET (b) Symbol

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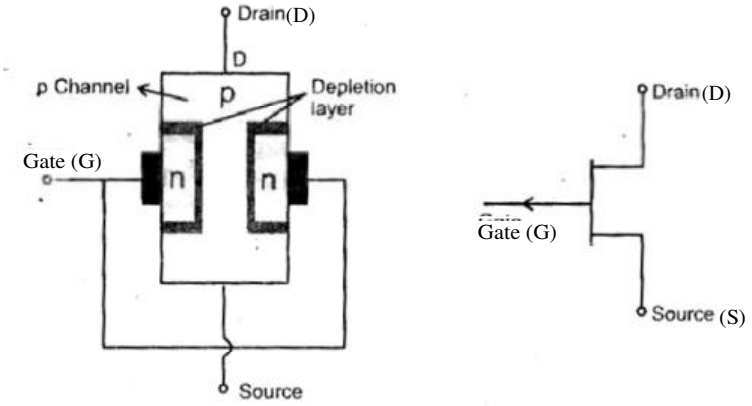

Fig 3.2 (a) p Channel JFET **(b) Symbol**

* n - Channel JFET consists of n type silicon bar called as "**CHANNEL**"

* 2 pieces of p-type material are attached to its sides forming *pn* junctions.

* Channel ends are **SOURCE (S) and DRAIN (D)**

SOURCE → terminal through which majority carriers enters the bar.

DRAIN → terminal through which majority carriers leave the bar.

* 2 p-regions are formed **by alloying** or **by diffusion** and connected together. Terminal is called **GATE**. Christo Ananth et al.[1] discussed about principles of Semiconductors which forms the basis of Electronic Devices and Components. Christo Ananth et al. [2] discussed about Improved Particle Swarm Optimization. The fuzzy filter based on particle swarm optimization is used to remove the high density image impulse noise, which occur during the transmission, data acquisition and processing. The proposed system has a fuzzy filter which has the parallel fuzzy inference mechanism, fuzzy mean process, and a fuzzy composition process. Christo Ananth et al.[3] presented a brief outline on Electronic Devices and Circuits which forms the basis of the Clampers and Diodes.

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OPERATION OF n - CHANNEL JFET : (Nov /Dec 2012 - 8 Marks)

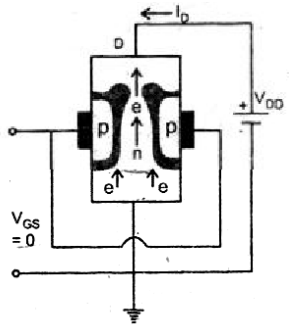

Fig 3.3 (a)

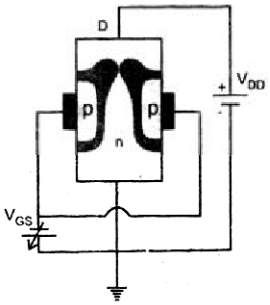

Fig 3.3 (b)

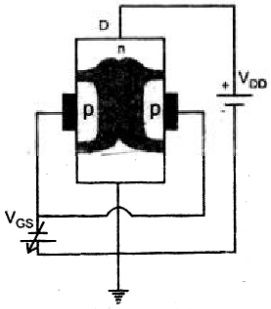

Fig 3.3 (c)

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1) **When V_{DS} - fixed positive value and reverse bias on V_{GS} is increasing:**

* Let Gate → **not biased** and fixed positive voltage is applied between drain and source terminals.

* So Electrons will move through n- type channel from source to drain.

* When Gate →**negative biased**, *pn* junctions are reverse biased and depletion regions are formed.

* Channel is **lightly doped** ⇒ Depletion region penetrates deeply into channel

⇒ Effective channel width is reduced

⇒ Increase in channel resistance and reduction in drain current I_D.

2. V_{GS}= 0; V_{DS} is varied:

* Let V_{GS}= 0, When V_{DS} = 0, Current flowing through FET is 0 ((i.e,) I_D= 0)

* Channel between drain and source acts as resistance.

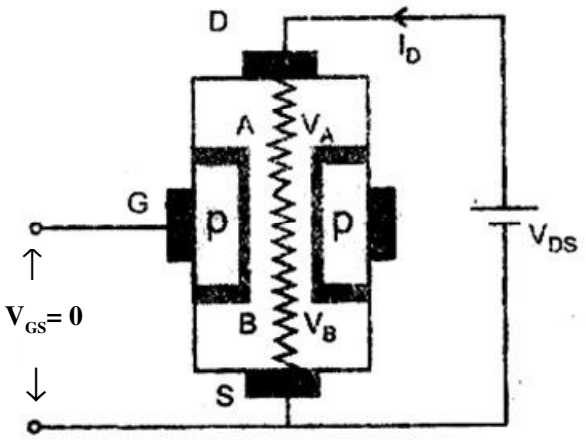

Fig 3.4 (a) n -CHANNEL JFET: CHANNEL REHAVING AS RESISTOR

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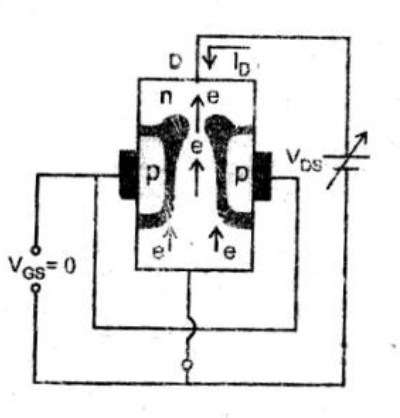

Fig 3.4 (b)

Fig 3.4 (a), (b) n - Channel JFET: Channel behaving as Resistor

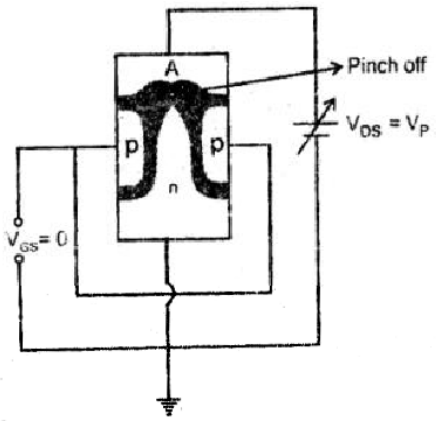

Fig 3.5 V_{GS}=0 and V_{DS} is varied

* Drain current I_D flowing through channel causes voltage drop between drain and source.

* Voltage at point A > Voltage at point B

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* Upper region of p-type material is more reverse biased than lower region.

* Width of depletion region near top of p-material > Width of depletion region near bottom of p-material.

* As V_{DS} is increased ⇒ Increase in reverse bias ⇒ Increase in width of depletion region.

* When channel is pinched off, conduction is blocked.

* Drain to source voltage at which I_D reaches I_{DSS} (Drain - source saturation current) is called "**PINCH OFF VOLTAGE (V_p)**"

* If V_{DS} is increased beyond V_p, I_D remains same and JFET acts as current source.

* If V_{DS} is further increased, a stage is reached at which gate - channel junction breaks down due to avalanche effect. At this point, drain current increases rapidly and device may be destroyed.

CHARACTERISTICS OF JFET: (May /June - 2014 - 8 Marks)

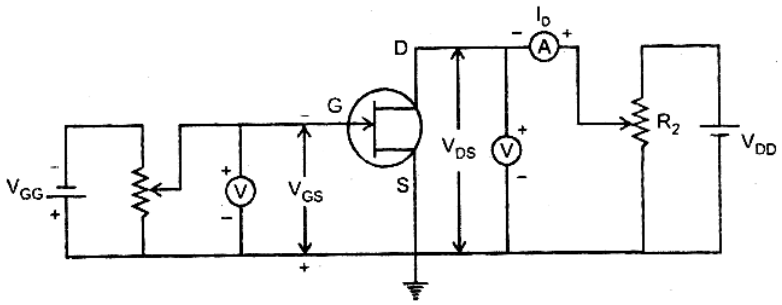


Fig 3.6 CHARACTERISTICS OF JFET

1. DRAIN Characteristics (Relation between I_D and V_{DS} for different values of V_{GS})

2. TRANSFER Characteristics (Relation between I_D and V_{GS} for constant V_{DS})

x

3.2 JFET DRAIN CHARACTERISTICS:

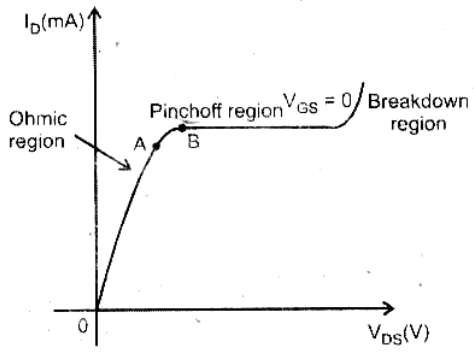


Fig 3.7 DRAIN CURRENT Vs DRAIN - SOURCE VOLTAGE (V_{GS} =0)

* Gate to source Voltage (V_{GS}) is kept at 0 and V_{DS} is varied from 0.

* When V_{DS} = 0, drain current I_D is also zero.

* When V_{DS} is increased, drain current starts flowing through channel and FET behaves like resistor till point A.

* Portion of characteristics where FET behaves like resistor is called "**OHMIC REGION**". FET can be used as "**VOLTAGE VARIABLE RESISTOR**" in ohmic region. **(May /June - 2014 - 2 Marks)**

* If V_{DS} is increased, a stage is reached at which pinch off occurs and drain current reaches saturation level.

* Drain to source voltage (V_{DS})at which pinch off occurs → **PINCH OFF VOLTAGE (V_p)** and corresponding I_D is known as I_{DSS}

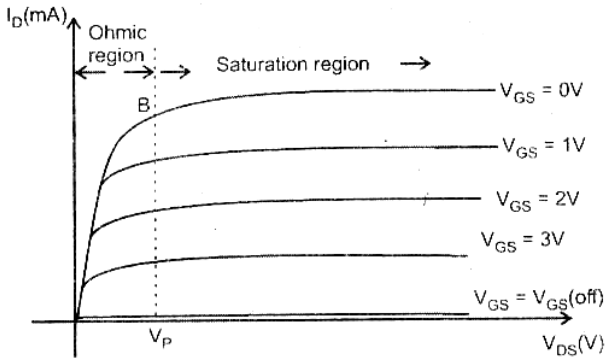


Fig 3.8 Drain current Vs Drain - source voltage (For different values of V_{GS})

* Even if V_{DS} is increased above V_p, drain current does not increase.

* Region where drain current is constant inspite of variation in V_{DS} is called "**PINCH OFF REGION**"

x

3.3 TRANSFER CHARACTERISTICS

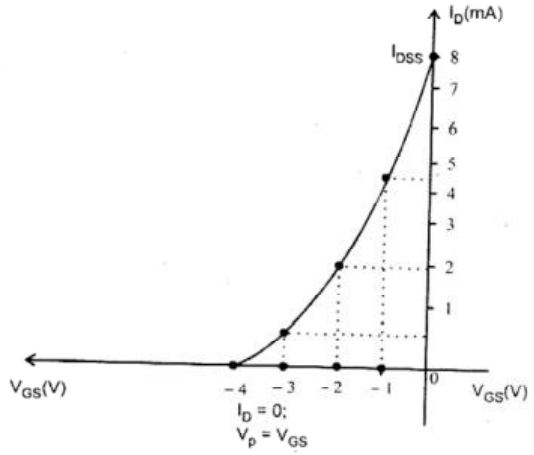


Fig 3.9 Transfer Characteristics

* Plot of drain current I_D Vs V_{GS} for constant values of V_{DS}.

* When $V_{GS} = 0$, current flowing through FET = I_{DSS}

* When $V_{GS} = V_{GS}(OFF)$, drain current =0

* The relation between V_{GS} (Gate to source voltage) and I_D (Drain current) is given by "**SHOCKLEY's EQUATION**"

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS}(OFF)}\right]^2$$

* When V_{GS} increases, Channel Width is reduced.

When V_{GS} (OFF) = V_p,

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_p}\right]^2$$

x

3.4 PARAMETERS OF JFET (Nov /Dec 2012 -4 Marks)

1. ac drain resistance
2. Transconductance
3. Current Amplification factor
4. Drain Conductance

1. ac DRAIN RESISTANCE (r_d)

* Ratio of change in drain source voltage to change in drain current at constant gate to source voltage.

$$\text{ac DRAIN RESISTANCE } r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=\text{constant}}$$

2. TRANSCONDUCTANCE (g_m)

* Ratio of change in drain current to change in gate - source voltage at constant drain - source voltage.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}\Big|_{V_{DS}=\text{constant}} \quad \text{mA/volts or micromho}$$

3. CURRENT AMPLIFICATION FACTOR (μ)

* Ratio of change in drain source voltage ΔV_{GS} to change in gate source voltage at constant drain current.

$$\text{Amplification Factor , } \mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}\Big|_{I_D=\text{constant}}$$

$$= \frac{\Delta V_{DS}}{\Delta V_{GS}}$$

$$= \frac{\Delta V_{DS}}{\Delta I_D}\frac{\Delta I_D}{\Delta V_{GS}}$$

$$\square = r_d g_m$$

$$\boxed{\square = r_d g_m}$$

Amplification Factor = ac Drain Resistance × Transconductance

4. DRAIN CONDUCTANCE (g_d)

* Reciprocal of drain resistance (r_d) is **DRAIN CONDUCTANCE (g_d)**

$$g_d = \frac{\Delta I_D}{\Delta V_{DS}}$$

3.5 Comparison Between FET and BJT (Nov /Dec -2012-2 Marks)

(Nov /Dec 2009 -2marks)(May/June-2014 -2Marks)

FET	BJT
* Only 1 kind of charge carriers are responsible for conduction. It depends only on majority carriers. * FET has 2 junctions⇒less noisy. * FET →Voltage controlled device. * Negative temperature coefficient. * No thermal breakdown * Easy to fabricate * Higher voltage gain	* Both holes and electrons are responsible for conduction of current. It depends on both majority and minority carriers. * BJT is noisy because of single junction. * BJT →current controlled device. * Positive temperature coefficient * Has thermal breakdown * Fabrication is difficult * Low voltage gain

x

3.6 EXPRESSION FOR DRAIN CURRENT (CURRENT EQUATIONS)

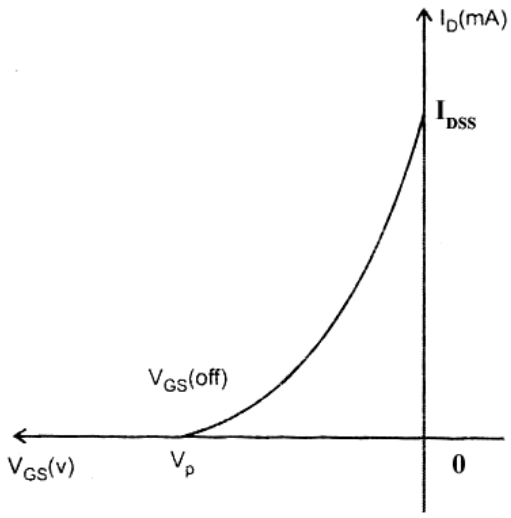


Fig. 3.10 TRANSFER CHARACTERISTICS OF JFET

* Drain source Voltage (V_{DS}) is kept constant and gate source voltage (V_{GS}) is varied.

* For different values of V_{GS}, drain current is plotted. V_{GS} is decreased from zero till I_D is reduced to 0.

From Shockley's equation,

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2 \rightarrow ①$$

where I_D = drain current

I_{DSS} = Value of I_D when $V_{GS} = 0$

V_P = Pinch off voltage

$$\frac{\partial I_D}{\partial V_{GS}} = I_{DSS}\left[2\left(1-\frac{V_{GS}}{V_P}\right)\left(\frac{-1}{V_P}\right)\right]$$

$$= \frac{-2I_{DSS}}{V_P}\left(1-\frac{V_{GS}}{V_P}\right)$$

We know that

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}=\text{constant}}$$

$$g_m = \frac{-2I_{DSS}}{V_P}\left(1-\frac{V_{GS}}{V_P}\right) \rightarrow ②$$

From①,

$$1-\frac{V_{GS}}{V_P} = \sqrt{\left(\frac{I_D}{I_{DSS}}\right)}$$

$$\therefore g_m = \frac{-2I_{DSS}}{V_P}\sqrt{\frac{I_D}{I_{DSS}}}$$

$$g_m = \frac{-2\sqrt{I_{DSS}\ I_D}}{V_P}$$

When $V_{GS} = 0$, $g_m = g_{m0}$

$$② \Rightarrow \therefore g_{m0} = \frac{-2\ I_{DSS}}{V_P}$$

$$\boxed{g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right)}$$

SLOPE OF TRANSFER CHARACTERISTICS AT I_{DSS}:

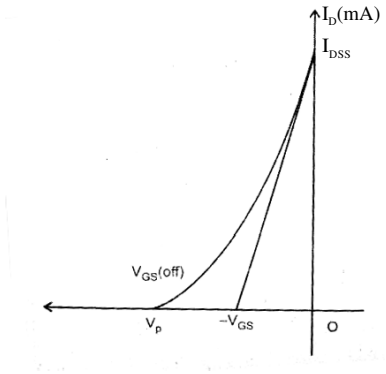


Fig.3.11 SLOPE OF TRANSFER CHARACTERISTICS

* To find slope of transfer characteristics at I_{DSS}, draw tangent line to characteristics at I_{DSS}

.

* Slope can be obtained by differentiating Shockley equation and then substitute

$$I_D = I_{DSS}$$

$$Slope = \frac{y_2 - y_1}{x_2 - x_1}$$

$$= \frac{I_{DSS} - 0}{0 - (-V_{GS})}$$

$$\text{Slope} = \frac{I_{DSS}}{V_{GS}}$$

Shockley's equation is

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

$$\frac{\partial I_D}{\partial V_{GS}} = \frac{-2I_{DSS}}{V_P}\left(1-\frac{V_{GS}}{V_P}\right)$$

$$= \frac{-2I_{DSS}}{V_P}\sqrt{\frac{I_D}{I_{DSS}}}$$

Substitute $I_D = I_{DSS}$

$$\frac{\partial I_D}{\partial V_{GS}} = \frac{-2I_{DSS}}{V_P} = \frac{I_{DSS}}{(-V_P/2)}$$

* To find the value of pinch - off voltage, tangent is drawn to current at $I_D = I_{DSS}$ and its intercept is found for 2 times on V_{GS} axis which is equal to V_P.

APPLICATIONS OF JFET (May / June 2014-6Marks)

→ **FET** →high input impedence which is used as input circuit for **instrument and audio applications.**

→ **Voltage Variable Resistor** in amplifiers

→**Level shifter** between 2 operational amplifiers operating at different supply voltages.

→ **nixie** tube drivers

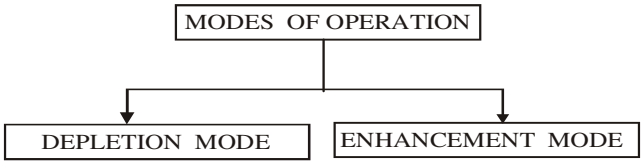
x

3.7 MOSFET (METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR

→ 3 terminal device (source, gate, drain)

→ Gate of MOSFET is insulated from channel. So MOSFET is also known as "**IGFET**"(Insulated gate FET)

→ no pn structure; Gate of MOSFET is insulated from channel by SiO_2 layer.



(Bias Voltage on gate reduces no. of charge carriers in channel. ⇒Decrease in drain current)

(Bias Voltage on gate increases no. of charge carriers in channel ⇒Increase in drain current)

DEPLETION MOSFET (D- MOSFET) (Nov / Dec -2010 - 8 Marks) (May/ June - 2012 - 2 Marks) (Nov/Dec -2009 - 8 Marks) (May /June - 2010- 8 Marks)

* Operate in both depletion and enhancement modes.

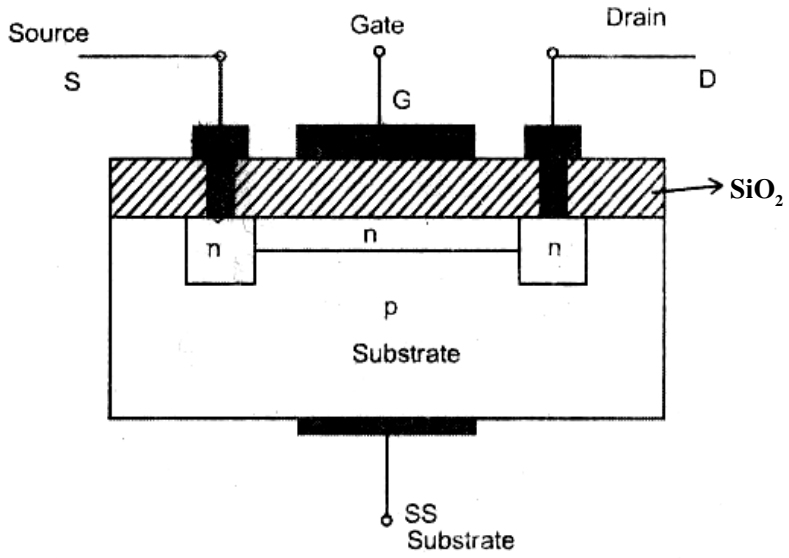


Fig 3.12 n -CHANNEL DEPLETION MOSFET

* It consists of lightly doped p- type substrate in which two highly doped n- regions are diffused. Two heavily doped n-regions act as Source and Drain.
* Lightly doped n-type channel is introduced between 2 heavily doped source and drain.
* Thin layer (of 1 □ m thickness) if SiO_2 is coated on the surface.
* Holes are cut in oxide layer to make contact with 'n' regions.

* Due to SiO_2, gate is completely insulated from channel.
* In some MOSFET's, p - type substrate is internally connected to source, whereas in many discrete devices, additional terminal is provided for substrate labeled SS.

A) BASIC OPERATION OF D-MOSFET

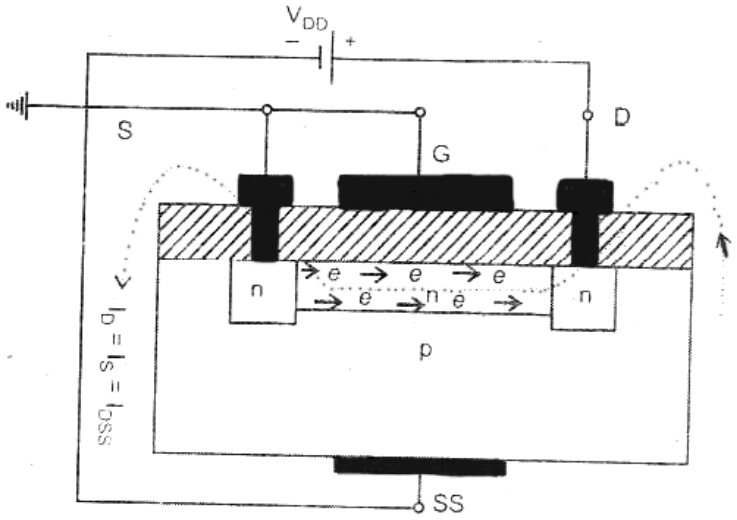


Fig . 3.13 n - CHANNEL DEPLETION MOSFET with $V_{GS} = 0$ AND APPLIED VOLTAGE V_{DD}

* Voltage V_{DS} is applied between drain and source terminal and V_{GS} =0
* Therefore, current is established from drain to source similar to JFET. Saturated drain current I_{DSS} flows during pinchoff.
* If negative voltage is applied to gate w.r.t source, holes are introduced in channel.
* Holes recombine with electrons and reduce no. of free electrons in n- channel available for conduction.
* Negative bias $\Rightarrow$less no. of free electrons in channel
* Negative voltage on gate deplete the channel, so the device is called "**DEPLETION MOSFET**"

* When sufficient negative voltage is applied to gate, channel may be completely cutoff and corresponding V_{GS} is called "**V_{GS} (OFF)**"
* If positive voltage is applied to gate w.r.t. source, electrons are induced in channel. Induced electrons constitute additional current from source to drain.
* If V_{GS} is increased more in positive direction, more no.of electrons are induced⇒ Increase in drain current.
* Mode in which MOSFET operates for positive values of gate - to - source voltage →"**ENHANCEMENT MODE**"

B) CHARACTERISTICS OF DEPLETION MOSFET

(1) DRAIN CHARACTERISTICS:

→ Plot of drain current Vs Drain - source Voltage for various values of Gate- Source Voltage.

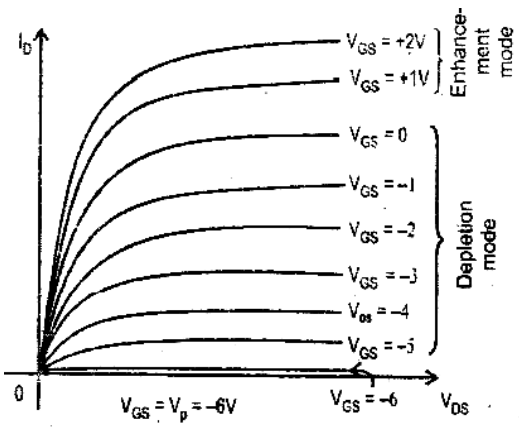


Fig 3.14 I_D Vs V_{DS}

→ For negative value of V_{GS}, characteristics of depletion MOSFET is similar to N- Channel JFET.

→ If Gate is made positive, additional carriers are introduced in channel and **CHANNEL CONDUCTIVITY** increases.

C) TRANSFER CHARACTERISTICS:

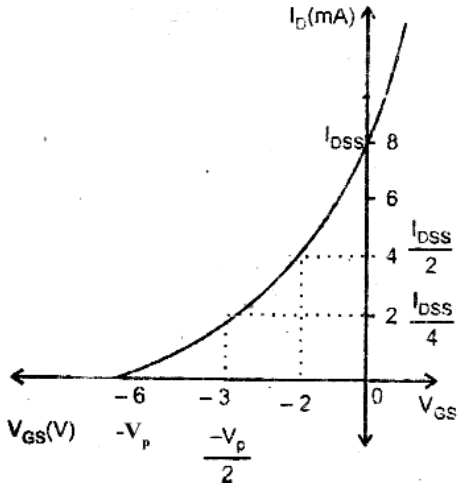


Fig 3.15 I_D Vs V_{GS}

* Depletion MOSFET can be operated with $V_{GS} > 0$

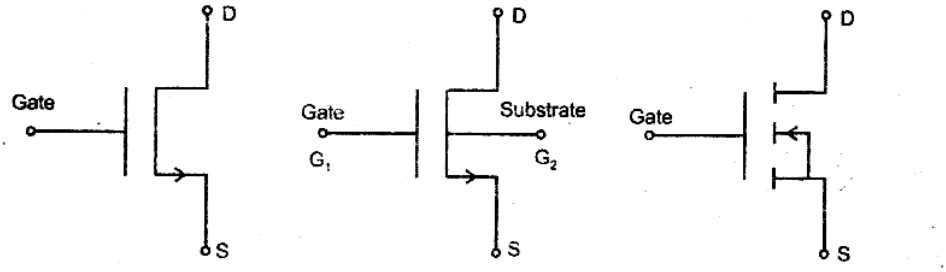


Fig 3.16 CIRCUIT SYMBOLS FOR n -CHANNEL MOSFET

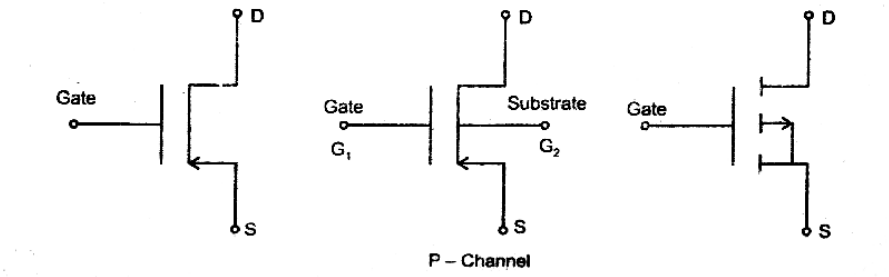


Fig 3.17 CIRCUIT SYMBOLS OF p CHANNEL MOSFET

ENHANCEMENT MOSFET (May/June - 2011 - 8 Marks) (May/June - 2010 - 8 Marks)(Nov / Dec -2010 - 8 Marks) (Nov/Dec -2009 - 8 Marks) (May /June - 2012- 2 Marks)

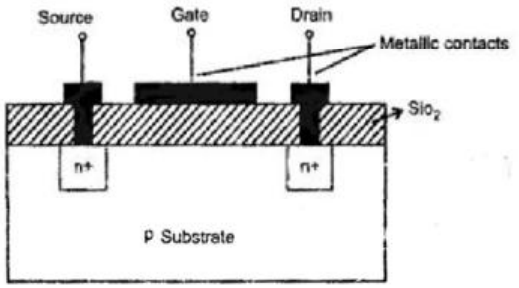


Fig. 3.18(a)

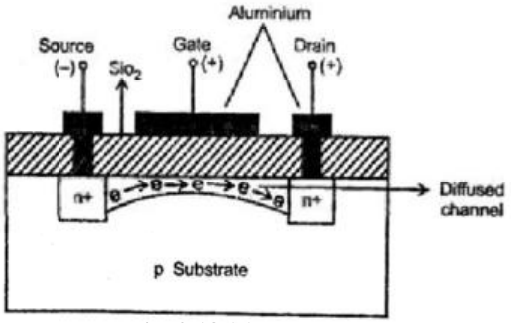


Fig. 3.18 (b)

Fig 3.18 (a), (b) WORKING OF n - CHANNEL ENHANCEMENT MOSFET

* It consists of p-type substrate and 2 heavily doped n-regions that act as source and drain (similar to **DEPLETION MOSFET**)

* SiO_2 layer isolates gate from region between drain and source.
* Source and drain terminals are connected through metallic contacts to n-doped regions.
* Enhancement MOSFET **does not contain** diffused channel between source and drain.

WORKING:

* When drain is made positive w.r.t source and no potential is applied to gate, a small drain current **((i.e) a reverse leakage current)** flows.
* If positive voltage is applied to gate w.r.t source and substate, negative charge carriers are induced in substrate.
* Negative charge carriers (MINORITY CARRIERS) in p substrate form **"INVERSION LAYER"**
* As gate potential is increased, more and more negative charge carriers are induced.
* Negative carriers that are accumulated between source and drain constitute n-type channel.
* Drain current flows from source to drain through induced channel.
* Magnitude of drain current depends on Gate potential.
* Conduction of channel is enhanced by positive bias voltage on gate, so the device is known as **"ENHANCEMENT MOSFET"**

A) DRAIN CHARACTERISTICS

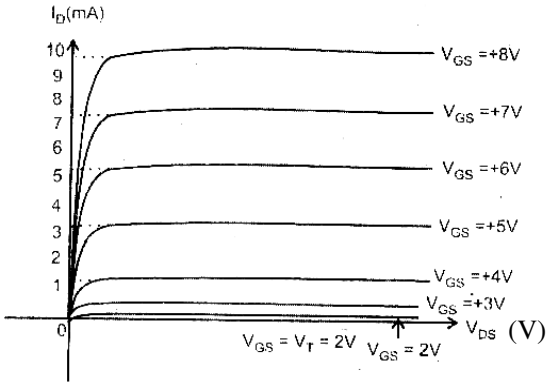


Fig 3.19 DRAIN CHARACTERISTICS

* I_{DSS} for $V_{GS} = 0$ is very small (nA)
* Drain current increases with positive increase in gate source bias voltage.

B) TRANSFER CHARACTERISTICS:

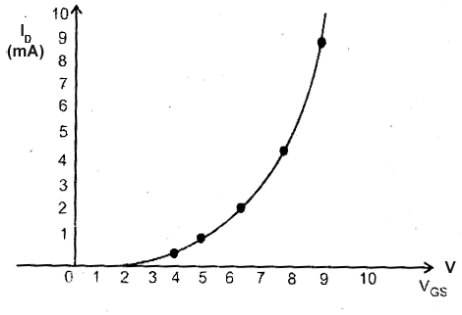


Fig 3.20 TRANSFER CHARACTERISTICS

* As V_{GS} is made positive, current I_D increases slowly and then more rapidly with increase in V_{GS}.
* Gate source Voltage at which there is significant increase in drain current is called **THRESHOLD VOLTAGE** (V_T or $V_{GS(th)}$)

C) EQUATION FOR TRANSFER CHARACTERISTICS:

$$I_D = k(V_{GS} - V_{GS\ (th)})^2$$

COMPARISON BETWEEN JFET AND MOSFET (Nov /Dec -2010 - 2Marks)

JFET	MOSFET
→ Input resistance is of the order of $10^9\ \Omega$ because no insulating layer is present between gate and conducting channel.	→ Input resistanceis very high in order of $10^{13}\ \Omega$ because insulation layer is present between gate and conducting channel.
→Gate leakage current is of order of 0.1 to 10mA	→ Gate leakage current is of order of 0.1 to 10pA
→ Drain resistance is of order of 0.1 to 1M Ω .	→ Drain resistance is of order of 1 to 50 K Ω
→ Operates only in depletion mode.	→ Operates both in enhancement and depletion modes
→ Electric field across reverse biased pn junction controls Conductivity of channel	→ Electric field across insulating layer controls Conductivity of channel.

3.9. **COMPARISON BETWEEN N- CHANNEL AND P-CHANNEL MOSFETs**

P-CHANNEL MOSFET	N- CHANNEL MOSFET
* Occupies 2 times more area than n- channel MOSFET	* Occupies 2 times less area than p- channel MOSFET
* Packing density of p-channel MOSFET is less than n- channel MOSFET.	* Packing density of n- channel MOSFET is more than p- channel MOSFET
* Slower than n- channel MOSFET	* Faster than p-channel MOSFET.
* p-MOS devices are bigger than n- MOS devices.	* n- MOS devices are smaller than p-MOS devices

3.10 **COMPARISON BETWEEN p-CHANNEL JFET AND n-CHANNEL JFET (May /June 2010 - 2Marks)**

p - Channel JFET	n - channel JFET
* Current carriers → holes	* Current carriers → electrons
* Channel is made of p-type material and gate of n-type material.	* Channel is made of n-type material and gate of p- type material.
* Symbol has arrow pointing away from drain / source channel.	* Symbol has arrow pointing towards drain / source channel.
* More noise produced	* Less noise produced
* Less Transconductance	* Large transconductance

X

3.11 THRESHOLD VOLTAGE OF MOSFET:

* **DEFINITION : Threshold Voltage** is defined as the applied gate Voltage required to achieve threshold inversion point. Christo Ananth et al. [4] discussed about PN junction diode, Current equations, Diffusion and drift current densities, forward and reverse bias characteristics and Switching Characteristics of Semiconductor Diodes. Christo Ananth et al.[5] analyzed NPN, PNP Junctions, Early effect, Current equations, Input and Output characteristics of CE, CB CC, Hybrid -π model, h-parameter model, Ebers Moll Model, Gummel Poon-model and Multi Emitter Transistor in Bipolar Junctions.

* **Threshold inversion point is** defined as the condition when surface potential is $\square_s = 2\square_{fp}$ for p- type semiconductor & $\square_s = 2\square_{fn}$ for n - type semiconductor.

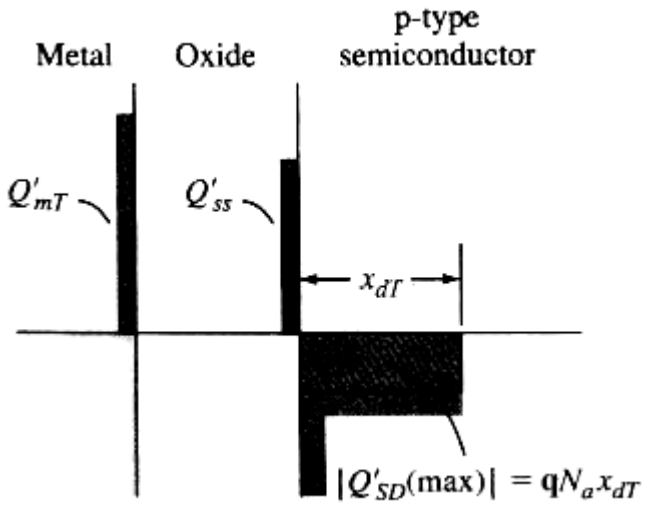


Fig 3.21 CHARGE DISTRIBUTION THROUGH MOS DEVICE AT THRESHOLD INVERSION POINT FOR p- TYPE SEMICONDUCTOR SUBSTRATE

* Equivalent oxide charge $\rightarrow Q'_{SS}$
* Positive charge on metal plate at threshold $\rightarrow Q'_{mT}$

$$Q'_{mT} + Q'_{SS} = \left|Q'_{SD}(\max)\right|$$

where $\left|Q'_{SD}(\max)\right| = qN_a x_{dT}$

$\left|Q'_{SD}(\max)\right| \rightarrow$ magnitude of maximum space charge density per unit area of depletion region.

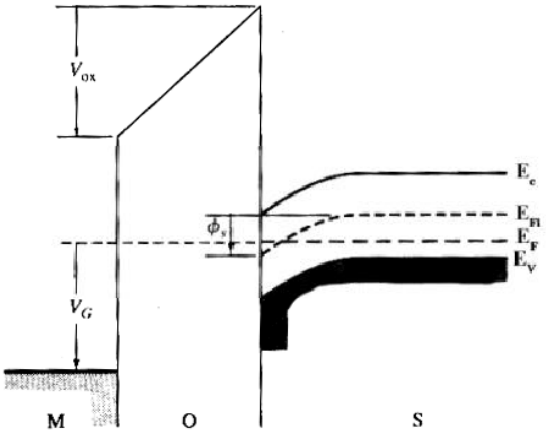


Fig 3.22 ENERGY BAND DIAGRAM THROUGH MOS STRUCTURE WITH POSITIVE APPLIED GATE BIAS

* Applied gate Voltage will change voltage across oxide and will change surface potential.

Gate Voltage $V_G = \Delta V_{OX} + \Delta \square_s$

$= V_{OX} + \square_s + \square_{ms}$

At threshold, $V_G = V_{TN}$ ($V_{TN} \rightarrow$ threshold voltage which creates electron inversion layer charge.)

Surface potential $\square_s = 2\square_{fp}$ at threshold

$$\therefore V_{TN} = V_{OXT} + 2\square_{fp} + \square_{ms}$$

where V_{OXT} is Voltage across oxide at threshold inversion point.

* V_{OXT} is related to charge on metal (Q'_{mT})and oxide capacitance (C_{OX})

$$V_{OXT} = \frac{Q'}{C_{mT}}$$

$$V_{OXT} = \frac{Q'_{mT}}{C_{OX}} = \frac{1}{C_{OX}}(|Q'_{SD}(\max)| - Q'_{SS})$$

Threshold Voltage

$$V_{TN} = -\frac{|Q'_{SD}(\max)|}{C_{OX}} - \frac{Q'_{SS}}{C_{OX}} + \square_{ms} + 2\square_{fp}$$

(or)

$$V_{TN} = (|Q'_{SD}(\max)| - Q'_{SS})\frac{t_{OX}}{C_{OX}} + \phi_{ms} + 2\phi_{fp}$$

* **Flat Band Voltage** is defined as applied gate Voltage such that there is no band bending in semiconductor. So there is zero net space charge in the region.

$$V_{FB} = \phi_{ms} - \frac{Q'_{SS}}{C_{OX}}$$

$$\therefore V_{TN} = -\frac{Q'_{SD}(\max)}{C_{OX}} + V_{FB} + 2\phi_{fp}$$

* Negative Voltage must be applied to gate to make inversion layer charge equal to zero; Positive gate Voltage will induce larger inversion layer charge.

* For p-side,

$$V_{TP} = \left(-|Q'_{SD}(\max)| - Q'_{SS}\right)\left|\frac{t_{ox}}{C_{ox}}\right| + \varphi_{ms} - 2\varphi_{fn}$$

where $\phi_{ms} = \phi_m - \left(\chi' + \frac{E_g}{2q} - \phi_{fn}\right)$

$|Q'_{SD}(\max)| = q N_d x_{dT}$

where $x_{dT} = \left[\frac{4\varepsilon_s \phi_{fn}}{qN_d}\right]^{1/2}$

$$\phi_{fn} = V_t \ln\left|\frac{N_d}{n_i}\right|$$

$V_{TP} \rightarrow$ threshold voltage which induces inversion layer of holes.

X

3.12 CHANNEL LENGTH MODULATION OF MOSFET :

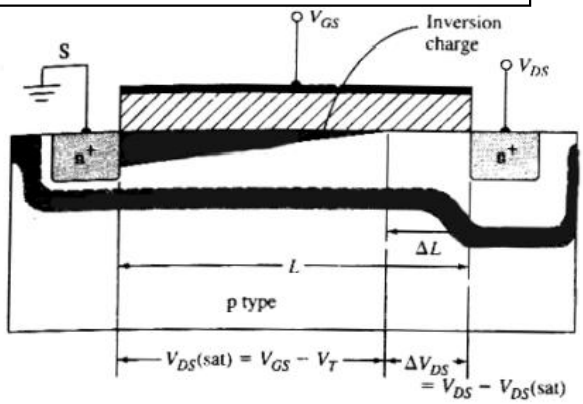


Fig 3.23 n - CHANNEL MOSFET showing CHANNEL LENGTH MODULATION EFFECT

Depletion Width extending into p-region of pn junction (under zero bias)

$$x_p = \frac{2\varepsilon_S \phi_{fp}}{qN_a}$$

Space charge width of Drain - substrate junction $x_p = \frac{2\varepsilon_S}{qN_a}(\phi_{fp} + V_{DS})$

* Space charge region defined by ΔL does not form until $V_{DS} > V_{DS}$ (sat)
ΔL = Total space charge width - Space charge width when $V_{DS} = V_{DS}$(sat)

$$\Delta L = \sqrt{\frac{2\varepsilon_S}{qN_a}}\left(\sqrt{\phi_{fp} + V_{DS}(sat) + \Delta V_{DS}} - \sqrt{\phi_{fp} + V_{DS}(sat)}\right)$$

where $\Delta V_{DS} = V_{DS} - V_{DS}$ (sat)

Electric field $E_{sat} \rightarrow$ electric field at the point where inversion layer charge is pinched off.

$$\frac{dE}{dx} = \frac{\rho(x)}{\varepsilon_S}$$

where $\rho(x) = -qN_a$
Integrating this equation,

$$E = \frac{-qN_a x}{\varepsilon_S} = -E_{sat}$$

Potential $\square(x) = -\int E dx$

$$= \frac{qN_a x^2}{2\square_S} + E_{sat}\ x + C$$

where C $\rightarrow$ integration constant

* **BOUNDARY CONDITIONS :**

$$\square(x = 0) = V_{DS}(sat)$$

$$\square(x = \Delta L) = V_{DS}$$

Substituting the boundary conditions,

$$V_{DS} = \frac{qN_a(\Delta L)^2}{2\square_S} + E_{sat}(\Delta L) + V_{DS}(sat)$$

$$V_{DS} = (\Delta L)^2 \left[\frac{qN_a}{2\square_{DS}\,S}\right] + V_{DS}(sat)(\because Neglecting\ E_{sat})$$

$$(\Delta L)^2\left(\frac{qN_A}{2\square_S}\right) = V_{DS} - V_{DS}(sat)$$

$$(\Delta L) = \sqrt{\frac{2\xi_S}{qN_a}}\left(\sqrt{\varphi_{sat} + (V_{DS}\ \square_{DS}\ (sat)} - \sqrt{\varphi_{sat}}\right)$$

where $\square_{sat} = \frac{2\square_S}{qN_a}\left|\frac{E^2_{sat}}{2}\right|$

* Drain current is inversely proportional to channel length

$$\boxed{I'_D = \left(\frac{L}{L - \Delta L}\right) I_D}$$

$I'_D \rightarrow$actual drain current

$I_D \rightarrow$ideal drain current

* I'_D is a function of V_{DS} even though the transistor is biased in saturation region.

* When MOSFET dimensions becomes small, ΔL becomes large and Channel length modulation becomes very severe.

3.13 CURRENT EQUATIONS OF MOSFET

ASSUMPTION :

→ Current in channel is due to drift rather than diffusion.

→ There is no current through gate oxide

→Any fixed oxide charge is an equivalent charge density at oxide - semiconductor interface.

→Carrier mobility in channel is constant.

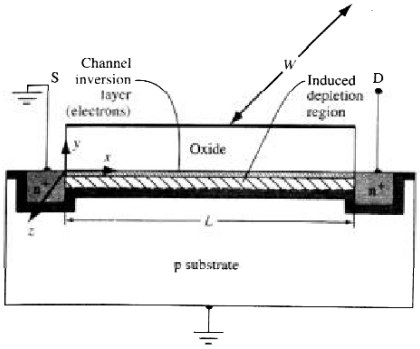


Fig 3.24 MOSFET STRUCTURE

By Ohm's law,

$J_x = \sigma E_x$

where σ → Channel Conductivity

E_x → Electric field along channel

$\sigma = q\mu_n n(y)$

where μ_n → electron mobility

n(y) → electron concentration in inversion layer.

Total channel current $I_x = \int_y \int_z J_x dy dz$

Inversion layer charge per unit area = $Q'_n = -\int q\, n(y)\, dy$

$I_x = -W\mu_n Q'_n E_x$

where W →Channel width

By charge neutrality:

$Q'_m + Q'_{SS} + Q'_n + Q'_{SD}(\max) = 0 \rightarrow ①$

where Q'_m →Charge on metal plate

Q'_{SS} →Equivalent oxide charge

$Q'_n \rightarrow$Inversion layer charge per unit area

$Q'_{SD(\max)} \rightarrow$maximum space charge density per unit area

By Gauss's law,

$$\oint_S \xi E_n dS = Q_T \qquad \rightarrow ②$$

where $Q_T \rightarrow$total charge enclosed by surface 'S'.

$E_n \rightarrow$normal component of electric field crossing surface 'S'.

$$\oint_S \xi E_n dS = -\varepsilon_{OX} E_{OX} W dx = Q_T \qquad \rightarrow ③$$

where $\varepsilon_{OX} \rightarrow$permittivity of oxide

Total charge enclosed $Q_T = \left[Q'_{SS} + Q'_n + Q'_{SD(\max)}\right] W dx$

$$\therefore -\xi_{OX} E_{OX} W dx = \left[Q_{SS}' + Q'_n + Q'_{SD(\max)}\right] W dx$$

$$-\varepsilon_{OX} E_{OX} = Q_{SS}' + Q_n' + Q'_{SD(\max)} \qquad \rightarrow ④$$

Fermi level in p-type semiconductor $\rightarrow E_{FP}$

Fermi level in metal $\rightarrow E_{FM}$

$$E_{FP} - E_{FM} = q(V_{GS} - V_x)$$

$$(V_{GS} - V_x) = V_{OX} + 2\varphi_{fp} + \varphi_{ms} \qquad \rightarrow ⑤$$

Electric field in oxide $E_{OX} = \dfrac{V_{ox}}{t_{ox}} \qquad \rightarrow ⑥$

$$④ \Rightarrow -\varepsilon_{OX} E_{OX} = Q_{SS}' + Q_n' + Q'_{SD(\max)}$$

$$= -\xi_{ox}\left[\frac{V_{ox}}{t_{ox}}\right] (\because \text{ from } ⑥)$$

$$= \frac{-\xi_{ox}}{t_{ox}}\left[(V_{GS} - V_x) - \varphi_{ms} - 2\varphi_{fp}\right] (\because \text{ from } ⑤)$$

$$= \frac{-\varepsilon_{ox}}{t_{ox}}\left[(V_{GS} - V_x) - (\varphi_{ms} + 2\varphi_{fp})\right]$$

We already know $I_x = -W\varphi_n Q_n' E_x$

$$I_x = -W\mu_n C_{ox} dV_x/dx\left[(V_{GS} - V_x) - V_T\right] \qquad \rightarrow ⑦$$

where $E_x = \frac{-dV_x}{dx}$

$V_T \rightarrow$threshold voltage

$= (|Q_{SD}'(max)| - Q_{SS}')\left\{\frac{t_{ox}}{\varepsilon_{ox}}\right\} + \phi_{ms} + 2\phi_{fp}$ (by threshold voltage equation)

From ⑦

Integrating ⑦,

$$\int_0^L I_x\, dx = -W\mu_n C_{OX} \int_{V_{x(0)}}^{V_{x(L)}} [(V_{GS} - V_T) - V_x]\, dV_x \qquad \rightarrow ⑧$$

The expression for drain current is

$$I_D = \frac{W\mu_n C_{OX}}{2L}\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right] \qquad \rightarrow ⑨$$

$$I_D(sat) = \frac{W\mu_n C_{OX}}{2L}\left[2(V_{GS} - V_T)V_{DS}(sat) - V_{DS}^2(sat)\right]$$

$$V_{DS} = V_{GS} - V_T$$

$$\therefore I_{D(sat)} = \frac{W\mu_n C_{OX}}{2L}\left[2(V_{GS} - V_T)(V_{GS} - V_T) - (V_{GS} - V_T)^2\right]$$

$$= \frac{W\mu_n C_{OX}}{2L}\left[2(V_{GS} - V_T)^2 - (V_{GS} - V_T)^2\right]$$

$$\boxed{I_D(sat) = \frac{W\mu_n C_{OX}}{2L}\left[(V_{GS} - V_T)^2\right]}$$

This is the ideal current equation in saturated region.

X

3.14 EQUIVALENT CIRCUIT MODEL AND ITS PARAMETERS:

* Source and substrate are both connected to ground potential.
* $C_{gs} \rightarrow$ gate to substrate pn junction capacitance.
* $C_{gd} \rightarrow$ gate to drain pn junction capacitance
* $C_{gsp} \rightarrow$ gate to substrate parasitic or overlap capacitance
* $C_{gdp} \rightarrow$ gate to drain parasitic or overlap capacitance $\rightarrow$lowers frequency response of device.

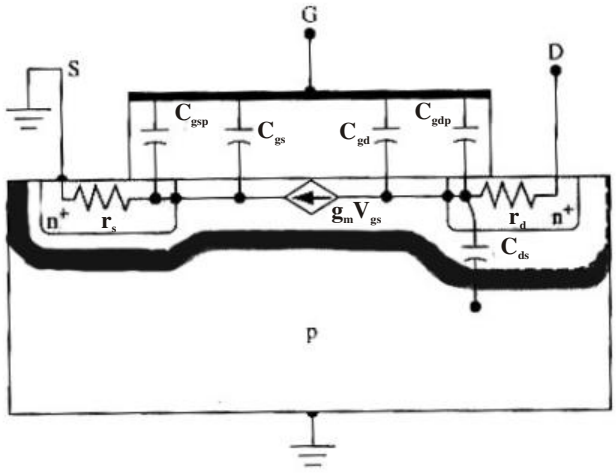


Fig 3.25 RESISTANCES AND CAPACITANCES IN n- CHANNEL MOSFET STRUCTURE

C_{ds} → drain - to - substrate pn junction capacitance

r_s, r_d → series resistances associated with source and drain terminals.

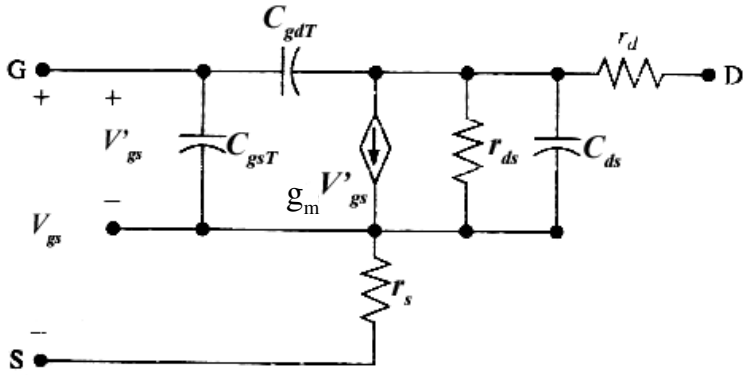


Fig 3.26 SMALL SIGNAL EQUIVALENT CIRCUIT

V_{gs} → Internal gate to source voltage which controls channel current

C_{gsT} →Gate to - source total capacitance

C_{gdT} →Gate - to - drain total capacitance

r_{ds} →drain - to source resistance which is associated with slope I_DVs V_{DS} .

* r_{ds} is finite because of Channel length modulation.

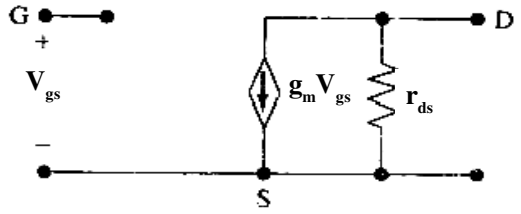


Fig 3.27 SIMPLIFIED SMALL - SIGNAL EQUIVALENT CIRCUIT

* Here r_s and r_d resistances are neglected, So Drain current is a function of gate - to - source voltage through transconductance.
* Input gate impedance→ infinite

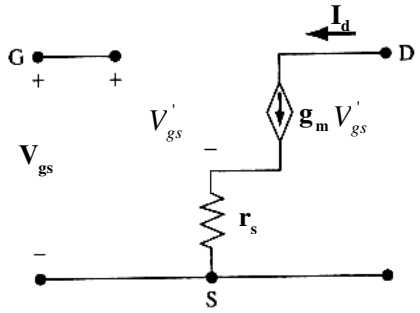


Fig 3.28 SMALL SIGNAL EQUIVALENT CIRCUIT INCLUDING SOURCE RESISTANCE r_s

* Here r_s is included and r_{ds} is neglected.

Drain current $I_d = g_m V'_{gs}$ →①

Relation between V_{gs} and V'_{gs} is

$$V_{gs} = V'_{gs} + [g_m V'_{gs}] r_s$$

$$\boxed{V_{gs} = [1 + g_m r_s] V'_{gs}} \rightarrow ②$$

Subs ② in ①

$$I_d = \frac{g_m V_{gs}}{1 + g_m r_s}$$

$$\boxed{I_d = g'_m V_{gs}} \rightarrow ③ \qquad \left(\because g'_m = \frac{g_m}{1 + g_m}\right)$$

* Equivalent circuit of *p* - channel MOSFET is just the same as *n*- channel MOSFET except that **Voltage polarities** and **current directions** are **reversed.**

X

3.14.1 PARAMETERS OF EQUIVALENT CIRCUIT MODEL:

1. VOLTAGE GAIN (A_V)

Voltage gain (A_V) = $\frac{V_0}{V_i}$

* Ratio of output voltage to input voltage → A_V

$$V_0 = -g_m V_{gs} (r_d \| R_D)$$

$$V_0 = -g_m V_i (r_d \| R_D) (\because V_{gs} = V_i = \text{input voltage})$$

$$\frac{V_0}{V_i} = -g_m \left(r_d \| R_D\right)$$

$$A_V = -g_m (r_d \| R_D)$$

If $R_D > r_d$,

$$\boxed{A_V = -g_m R_D}$$

2. INPUT IMPEDANCE (Z_i)

$$\boxed{Z_i = r_s}$$

3. OUTPUT IMPEDANCE (Z_0)

$$Z_0 = r_{ds} \| r_d$$

If $r_{ds} > r_d$

$$\boxed{Z_0 = r_{ds}}$$

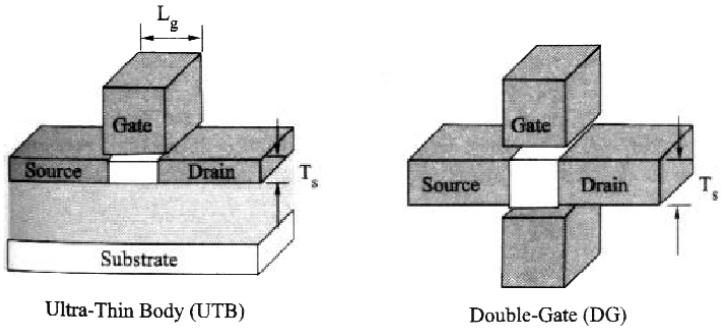
4. INPUT CAPACITANCE (MILLER CAPACITANCE)

$C_i = C_{gs} + (1 + g_m R'_d) C_{gd}$

x

3.15 FINFET (May/June-2014-4Marks)

* **FINFET** - Multiple gate field effect transistor (MUGFET) or a multiple device which incorporates more than one gate into single device.
* Multiple gates are controlled by single gate electrode.
* Multiple gate device employing independent gate electrodes = **Multiple Independent Gate Field Effect Transistor (MIGFET)**
* **"Fin"** - narrow channel between source and drain.
* The thin - body MOSFET structure **controls short channel Effects** and **suppresses leakage** by keeping gate capacitance in close proximity to channel.



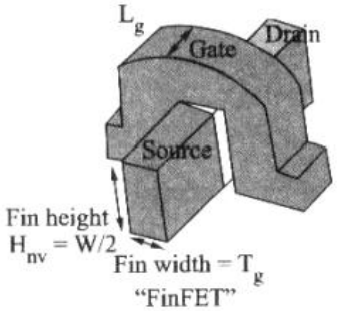


Fig 3.29 DOUBLE GATE FINFET DEVICE

* Planar Double gate MOSFET structure is rotated 90º to provide lowest gate leakage current and enables easy manufacturing using standard lithography techniques because gate electrodes are self - aligned.
* The Gate has control over conducting channel which allows very small leakage current when device is in OFF state.
* This results in low threshold voltages which results in greater switching speed.
* FINFETs → 37% faster than planar devices.
* FINFETs → balances throughput performance and power.

ADVANTAGES:

→ Improved frequency performance
→ Reduced capacitance
→ High drive current
→ Reduction in interconnect length
→ Minimizes Noise and latchup

DISADVANTAGES

→ Quantized widths
→ Bulk in size⇒ Problems of self Heating and dissipation of power.

x

3.16 DUAL GATE MOSFET (May/June -2014 - 4 Marks)

→ Dual Gate MOSFET or double gate transistor is an N-Channel enhancement type, dual - insulated gate FET which utilizes MOS construction.
→ Consists of 2 equal dual gate MOSFET with shared source and gate leads.
→ Source and substrate are interconnected.
→ Internal bias circuits enable DC stabilization and good cross - modulation performance during automatic Gain control.
→ The transistor has micro miniature plastic package.

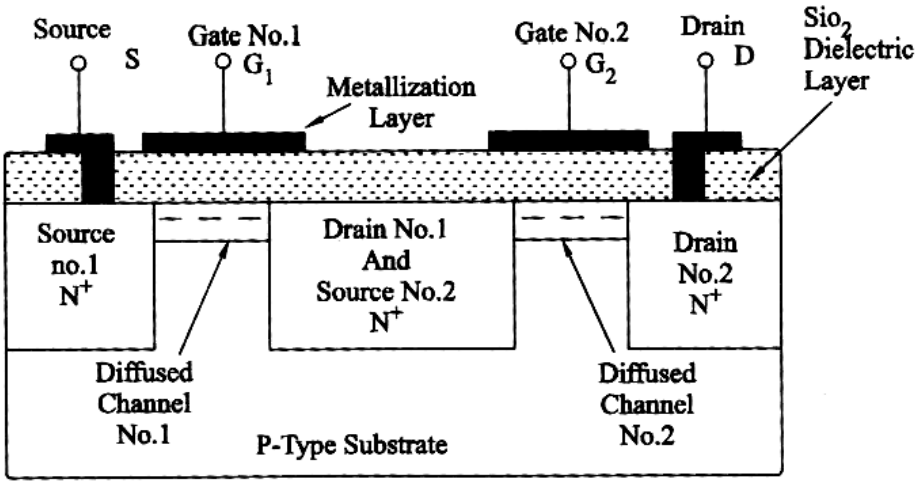


Fig 3.30 DUAL GATE N-CHANNEL DEPLETION MOSFET

* Dual - Gate MOSFET has tetrode configuration where both gates control the current in the device.
* Used for small - signal devices in RF applications.
* Biasing drain - side gate at constant potential reduces gain loss caused by Miller effect.
* Tetrode configuration does not replicate vacuum - tube tetrode.
* Vacuum - tube tetrodes exhibit lower grid plate capacitance and high output impedance with high voltage gain than triode Vacuum tubes.

3.16.1 SALIENT FEATURES

→ 2 AGC amplifiers in 1 package
→ High AGC - range, high gain, low noise figure.
→ Integrated gate protection diodes.

ADVANTAGES

* Better control over short channel effects.
* Advantageous over existing fabrication processes.
* High current driving capability
* Uniformity of Silicon channel thickness

DISADVANTAGES

→ Accessing bottom gate for device wiring is not easy.

→ Front and back gates cannot be independently biased.

→ Fabrication of back gate and gate dielectric below Silicon channel is difficult.

APPLICATIONS

→ 2 gain controlled input stage for UHF and VHF tuners.

→ Professional communication equipment.

X

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