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High Speed and Low Power ASIC Using Threshold Logic

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***Abstract* – In this paper, a new circuit architecture of a differential threshold logic gate called PNAND is proposed. The main purpose of this work to reduce the leakage, power and area of standard ASIC Circuits. By predicting the performance comparison of some electrical quantity such as charge, voltage or current, the implementation of threshold logic gates (TLG) is considered in this paper. Next a hybridization technique is done by replacing the flipflops and parts of their clocks with PNAND cells is Proposed. At last the proposed PNAND cell is hybridized with conventional logic cells, which will result in lower power consumption, leakage and area. This paper is proposed using Cadence® Virtuoso Schematic Editor at 180nm technology. Several design circuit methodologies such as retiming and asynchronous circuit design can used by the proposed threshold logic gate effectively.**

***Index Terms*— PNAND, ASIC, TLG.**

I. INTRODUCTION

The static differential threshold gates (DTGs) overcome the obstacles posed by dynamic flip-flops that embed NMOS logic. The main feature of a DTG flip-flop is computing and amplifying the conductivity difference between two networks of parallel transistors referred to as the left input network (LIN) and the right input network (RIN). If the LIN has lower impedance then the output is logic 1, otherwise it is 0. Since the impedance of either network is an integral multiple of the number of ON transistors, the Boolean function of such DTG can be described by the predicate $\sum xi > \sum yi$ where xi are variables controlling the number of ON transistors in the LIN and yi are Boolean variables controlling the number of ON transistors in the RIN. This predicate can be algebraically rearranged to yield the predicate $\sum(xi - yi) > 0$. This type of pseudo-Boolean predicate corresponds to the class of linear threshold functions. Given a linear threshold function (which is a Boolean function), it is possible to connect the variables (and constants) to the input networks such that predicate of the DTG reduces to that of the given threshold function. . However, threshold functions, which are a proper subset of unite Boolean functions, can be computed by fundamentally

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different mechanisms, and this presents the possibility of further improvements in power consumption, performance and area, which have not been thoroughly explored.

Let X=(x1,x2,….,xn), xi € {0,1}, w = (w1,w2,….,wn), wi € R, and T € R. A unate Boolean function f(X) is called a threshold function if there exist weights w and a fixed threshold T such that

f(X)= 1 if w'X ≥T

0 otherwise

Without loss of generality, the weights w and threshold T can be assumed to be positive integers.

A threshold function can be implemented in the same way as any logic function, e.g. network of logic primitives or a pull-up and pull-down network of pFETs and nFETs, etc. Such implementations are not considered here, as they offer nothing new, and in fact, can be quite inefficient for implementing threshold functions in terms of speed, power and area. By predicting the performance comparison of some electrical quanty such as charge, voltage or current, the implementation of threshold logic gates (TLG) is considered in this paper.. This is what distinguishes such implementations of a threshold gate with any of the conventional implementations of CMOS logic functions.

The reason for examining threshold gates as logic primitives stems from the fact that they are computationally more powerful than the standard AND/OR logic primitives. Many common logic functions such as the n-bit parity, n-bit multiplication, division, powering, sorting, etc,. can be computed by polynomial size threshold networks of a fixed number of levels, while the same would require exponential size AND/OR networks.

II. ARCHITECTURE

Figure 1.1 shows the schematic of the threshold gate with multiple inputs that can be named as k, henceforth referred to as PNAND-k cells. The architecture consists of three main components: (1) two groups of parallel pFET transistors referred to as the left input network (LIN), and right input network (RIN), (2) a sense amplifier (SA), which consists of a pair of cross coupled NAND gates, and a (3) set-reset (SR) latch. The cell is operated in two phases:reset (CLK = 0) and evaluation (CLK 0 = 1).

Cell Operation: When clock sets to 0 the current will discharges through M8 and M19.It pull nodes N5 and N6 low, which turn off M5 and M6, and also disconnects all paths from N1 and

N2 to ground. . In other hand, the transistors M7 and M8 are active, which results in N1 and N2 being pulled high. The nFETs M3 and M4 are ON. the state of the SR latch does not change with the nodes N1 and N2 being high.

When CLK is sets to 1 an input that results in active devices in the LIN and r active devices in the RIN is denoted by l/r. The signal assignment procedure will ensure that $l \neq r$. Assume that $l > r$. As a result, the conductance of the LIN is higher than that of the RIN.As the discharge devices M18 and M19 are turned off, both N5 and N6 will rise to 1. Due to the higher conductivity of the LIN, node N5 will start to rise first, which turns on M5. With M3 = 1, N1 will start to discharge through M3 and M5. The delay in the start time for charging N6 due to the lower conductance of the RIN allows for N1 to turn on M2 and turn off M4. Thus, even if N2 starts to discharge, its further discharge is impeded as M2 turns on, resulting in N2 getting pulled back to 1. As a result, the output node N1 is 1 and N2 is 0. As the circuit and its operation are symmetric, if $l < r$, then the evaluation will result in N1 = 0 and N2 = 1.

The active low SR-latch stores the signals N1 and N2. During reset, when (N1,N2) = 1, the SR-latch retains its state. After evaluation, if (N1,N2) = (0,1), the output Q = 0, and if (N1,N2) = (1,0), Q = 1, providing a dual-rail output for the threshold function being computed. Therefore, once evaluated after rising edge of the CLK, the output Q of the cell is stable for the remaining duration of the clock cycle. Hence, it operates like an edge-triggered flipflop, that computes a threshold function.

Since it is the difference in conductivity between the LIN and RIN that is sensed and amplified, the greater the difference, the faster and more reliably the cell operates. In the layout of the PNAND cell, several steps were taken to ensure robustness to process variations and signal integrity. A symmetric SR-latch was used to ensure near identical load on node N1 and N2 and near equal rise and fall delays. The source nodes of M16 and M17 are shorted so that the transistors in the LIN and RIN have nearly identical VD, VG and VS before clock rises.

The sizes of the pull-down devices in the differential amplifler were optimized, as were the sizes of the input transistors in the LIN and RIN to maximize the conductivity difference for the input combination that results in the worst-case contention between the LIN and RIN, while keeping the RC delay of the input networks as low as possible.

In addition, to further improve the robustness of the cell, an internal feedback is created with transistors M9 and M10 in the LIN and RIN, driven by N1 and N2, respectively.

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These additional transistors M9 and M10 in the input networks serve as keepers to avoid the situation where N5 and N6 might be in a high impedance states (HiZ1,HiZ0).

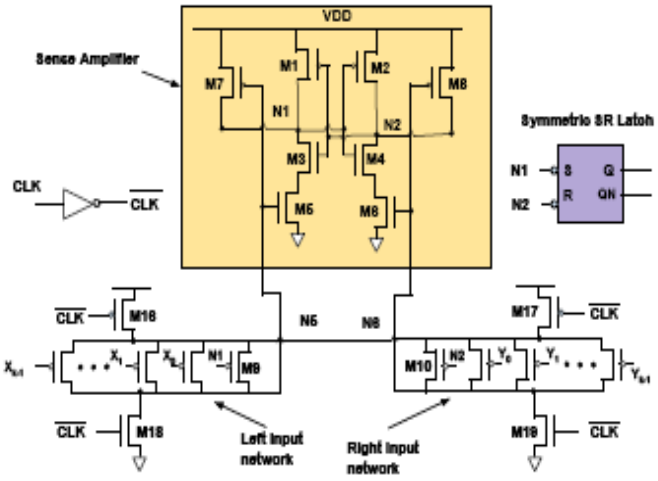

Fig 1.1 PNAND design cell

Assume for the moment that M9 and M10 are not present, and consider the situation in which there are k active devices in the LIN and none in the RIN. After reset, N5 and N6 are both 0. When the clock rises to 1, N5 will rise to 1, and N6 will be HiZ0, and the circuit will correctly evaluate with N1 = 0;N2 = 1. Note that M4 is inactive and M3 is active. Now suppose that while CLK = 1 the inputs change, and all transistors in the LIN become inactive and some k transistors in the RIN become active. N5 is now HiZ1, and N1 will remain at 0, keeping M4 inactive. However, N6 rises to 1, turning on M6, but as long as M4 remains inactive, and M2 active, no change will take place. N5, being HiZ1, is susceptible to being discharged. If that happens, N1 rises, activating M4, and discharging N2, which results in the output being complemented.

Transistors M9 and M10 ensure that N5 and N6 do not become HiZ0 or HiZ1. In the above situation, once N1 = 0 during evaluation, the presence of M9 driven by N1 ensures that N5 = 1. Hence, after evaluation and while CLK = 1, any change in the input state will not affect the side that determined the output, i.e. was discharged first, and hence the output will not be disturbed.

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III. SCAN IMPLEMENTATIONS

The PNAND cell is a multi-input flip-flop, therefore it is necessary for it to have typical features of a D-flipflop such as asynchronous preset and clear as well as scan. Evidently the PNAND cell operates quite differently compared to a master-slave D-flipflop

If PNAND cells are to replace flipflops and clocks, scan capability is essential. The simplest way to make a D-FF scannable is to use a 2:1 mux that selects between the input D and the test input (TI), depending on whether or not the test mode is enabled (TE). This is not practical for a multi-input flip-op like the PNAND cell. Although there exist several ways to implement scan for a PNAND cell, the one shown in Figure 1.2 has negligible impact on the cell's performance and robustness during normal operation. All other variations were significantly worse in this regard.

The additional transistors for scan are labeled as S1 through S6. In the normal mode, the signals TE (test enable) and TI (test input) are both 0, which disables the scan related transistors (S1 through S4), and reduces the circuit function to the one shown in Figure 1.2.

In the scan mode, the TE signal itself acts as a clock for a PNAND. In fact regular clock CLK must be held 0 for the scanning mechanism to work. Therefore, if a circuit has a mix of D-FFs and PNAND cells, the PNAND cells must be part of a separate scan chain. A common TE signal is used for both the scan chains. However the way this TE signal is operated is different from the conventional scanning mechanism. First the signal TE is held high and data is scanned into regular flipflops (conventional way). Once this is finished, the CLK is held 0 and following procedure is performed to stored data bits in PNANDs. Signal GTI (global test input) is the entry point for the scan data input to the PNAND chain.

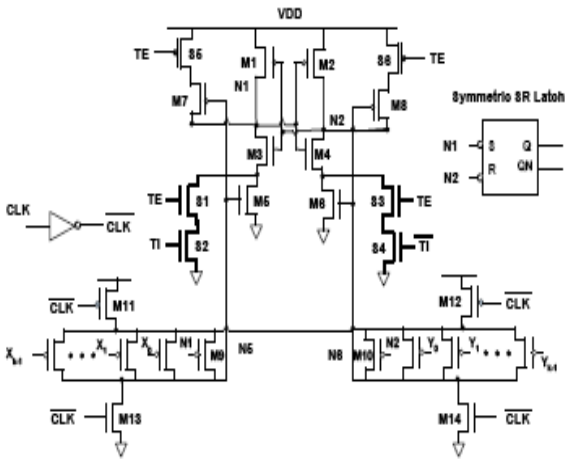

Fig 1.2 PNAND Cell Design with Scan

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However the way this TE signal is operated is different from the conventional scanning mechanism. First the signal TE is held high and data is scanned into regular flipflops (conventional way). Once this is finished, the CLK is held 0 and following procedure is performed to stored data bits in PNANDs. Signal GTI (global test input) is the entry point for the scan data input to the PNAND chain.

1. Set CLK = 0 and TE = 0.
2. Set GTI = i'th bit of the input (i = 0 initially).
3. Set TE = 1. Each PNAND registers its TI input.
4. Set TE = 0.
5. Increment i and repeat until the end of stream.

Note that as long as CLK = 0, the toggling of TE signal alone does not alter the data already stored in the conventional D-Flipflop scan chain. Therefore at the end of this procedure both PNANDs and flipflops store the required set of bits and regular clocking can proceed. The pullup transistors S5 and S6 are included to eliminate a DC path during testing. In absence of these transistors, when TE is asserted (0 → 1), while CLK = 0, M7 is active, and there is a DC path V DD →M7 → M3 S1 → S2 → GND. Fig. 3.5 shows the waveforms obtained via SPICE simulation of a scan chain of four PNAND-9 cells. The CLK is set to 0. The nodes Q1, Q2, Q3 and Q4 are output nodes of 4 cells that are initialized to 0. The scan pattern being registered is (Q1, Q2, Q3, Q4) = 1010.

IV. HYBRIDIZATION

In hybridization technique, the PNAND cell is incorporated into the conventional logic cells referred as ASIC circuits. By doing so we can reduce the area, leakage and power of that conventional cell without sacrificing their performance. It is the main advantage of designing the PNAND cell.

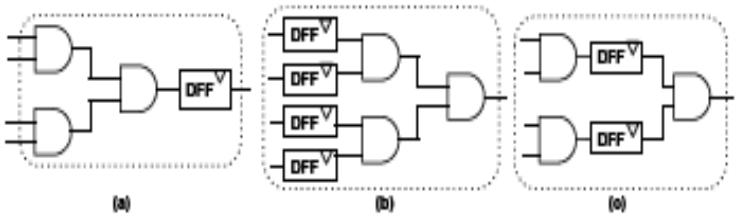

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Figure 1.3 Sub-circuits Replaceable by a Single PNAND cell

Replacing the ASIC Circuits with a single PNAND will reduce the total number of flip-flops in the resulting hybrid circuit, which may result in additional reduction in power.

V. CONCLUSION

This paper deals with the design of new, automated methodology for the design of digital ASIC circuits using a combination of conventional logic gates and threshold logic flip-flops. When the proposed threshold gates, operated at the nominal voltage, can be made robust in the presence of process variations.The schematic was designed in Cadence® Virtuoso Schematic Editor L 180 nm technology. The Schematic simulation and power analysis were done using Cadence® Virtuoso ADE L with 1.8 V as input. The power consumption was observed less than the existing system.

As the future work the sense amplifier and SR latch used to design the PNAND cell can be changed with the less number of transistors. By doing so the area and power consumption will further get reduced and also can propose clocking method called as local clocking to further improve power reduction of ASIC circuits. The most important thing about local clocking is that it provides incremental improvements to existing circuits. Therefore whether a circuit is already hybrid or not, local clocking can still be applied.

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