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IMPLEMENTATION OF NINE LEVEL ANPC CONVERTER USING ATmega8

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***Abstract*— This paper proposes a new modulation technique and a balancing control strategy for a single-phase nine-level flying-capacitor (FC)-based active-neutral-point-clamped (ANPC) converter. Here a multilevel power conversion concept based on the combination of neutral-point-clamped (NPC) and floating capacitor converters is used. In the proposed scheme, the voltage balancing across the floating capacitors is achieved by using a proper selection of redundant switching states, and the neutral-point voltage is controlled by the classical dc offset injection. The proposed modulator can control the FC voltage to follow the requested reference value and simultaneously generate the required ac output voltage regardless of the values of the dc capacitor voltages of the converter. By implementing this method, smaller values of the dc-link capacitor and FC can be used even in applications that could experience ripple or transient in the capacitor voltage. In a single-phase nine-level ANPC converter applications, where the capacitors can experience pulsation power and dc-link balancing issues, such as grid-connected photovoltaic system, the selection of the reference voltage value for the FC can play an important role to balance the average values of the dc-link capacitor voltage. Experimental results are illustrated in the paper to demonstrate the system operation. The proposed circuit is designed and analysed using MATLAB simulink.**

***Index Terms*— Active-neutral-point-clamped (ANPC) converter, flying capacitor (FC), photovoltaic (PV) power system, pulse width modulation, voltage balancing, Multilevel converters.**

I INTRODUCTION

Multilevel topologies provide a clever way of connecting switches in series, thus enabling the processing of voltages that are higher than the device rating. The industry need for medium voltage drives has triggered considerable research in this field, in which most applications include drives for pumps, blowers, compressors, conveyors, and the like. In general, multilevel converters are effective means of reducing harmonic distortion and dv/dt of the output voltages, which makes this technology applicable to utility interface and drives.

There are a limited number of topologies that provide multilevel voltages and are suitable for medium voltage applications. The most known topologies are the neutral-point-clamped (NPC), the flying capacitor (FC), and the cascaded H-bridge multilevel converters [3] [4] [5] [6]. Other topologies such as the hybrid converters have been proposed as well, but they are not fully accepted for industrial applications [7] [8].

The NPC multilevel converter shown in Figure 1(a) is a natural extension of the three-level converter presented by ANPC (NPC3L). As can be seen, the multilevel NPC converter requires multiple clamping points to synthesize the different voltage levels across the output. The disadvantage of multiple clamping points is a limitation on the maximum modulation index that is allowed with active power to assure voltage sharing across all the dc link capacitors [9]. Another drawback of the multilevel NPC converter is the need for series connection of the clamping diodes [10].

Figure 1(b) illustrates a five-level floating capacitor converter. By properly using the dc link and floating capacitor voltages, one can synthesize the required voltage levels across the output terminals. An interesting property of the floating capacitor converter is that the redundant switching states can be used to achieve proper voltage control across the floating capacitors. In general, the energy stored in the floating capacitors is a limiting factor to increasing the number of voltage levels, which makes the five-level approach the most practical for industrial applications. An increased number of voltage levels may only be practical from the view point of floating capacitor requirements if the

carrier frequency of the converter is increased. However, there are tradeoffs that should be observed between carrier frequency and switching losses in the converter.

The cascaded H-bridge multilevel converter shown in Figure 1(c) takes advantage of connecting single-phase

inverters in series that are fed by independent dc voltage sources. The approach can be extremely modular, and a stair- cased output voltage is produced by adding and/or subtracting the voltages of the single-phase modules. The power flow may be bi-directional if active front-end rectifiers are used in the single-phase modules. Although modular, the cascaded H-bridge multilevel converter requires a complex transformer to provide the various independent dc sources.

Based upon the previous description, this paper proposes an active neutral-point-clamped (ANPC) multilevel converter that combines the flexibility of the multilevel floating capacitor converter with the robustness of industrial NPC converters to generate multilevel voltages. The proposed concept is described and supported by simulation results, and experimental validation demonstrates the proposed technology.

The redundancy in the switching states of the FC-based ANPC converter allows the voltage across FC to be regulated. To generate the switching pulses, a variety of strategies have been presented to generate the output voltage with reduced harmonics and simultaneously regulate the FC voltage of the converter such as carrier-based pulse width modulation (PWM) [4], modified triangular carrier-based PWM [7], optimized pulse pattern [6] and selective harmonic elimination PWM [9], [10]. In these methods, to generate switching pulses, the dc-link capacitor voltages are considered balanced or the calculation is carried out based on balanced condition.

Space-vector PWM is used to generate switching pulses of three-phase five-level converters in [11]–[13]. Proper switching vectors between available redundancies are selected to control the FC voltages and to achieve balanced dc-link capacitor voltages. In [15] and [16], an optimum zero-sequence voltage is added to obtain balanced dc-link voltages. These methods are normally suitable for three-phase applications.

Although different techniques have been reported to control and generate switching pulses in the FC-based 9L-ANPC converter, most of these are mainly suitable for a three-phase application, and virtually, in all of these approaches, the dc-link capacitor voltages are considered balanced or controlled to be balanced. However, in some applications or under transient con- ditions, the dc-link capacitor voltages can experience voltage variation and also have a risk to become unbalanced.

In single- phase applications, where the dc-link capacitors can experience pulsation power and consequently ripple in their voltages, the ability to reduce the effect of voltage ripples on the dynamic behavior of the system is crucial. The ability to work under continuous ripple condition is considered desirable for the modulator. Furthermore, the dc-link capacitor voltage balancing is another problem encountered in single-phase applications, which cannot be solved using a three-phase technique such as adding zero-sequence voltage [15]. Applying unsymmetrical switching pattern in each half-cycle can overcome unbalancing problems; however, it will reduce the quality of the converter output. Moreover, in most single-phase applications, a dc-link voltage divergence problem can occur if the FC voltage is controlled to be a fixed value (a quarter of the dc-link voltage), as will be demonstrated in this paper.

II. PROPOSED CONVERTER CONCEPT

The proposed converter's block diagram is shown in Figure 2(a), which is named active-neutral-point-clamped nine-level (ANPC9L) converter. The proposed converter is an arrangement of four -level inverters connected in series is shown in figure 2(b). Two of such subsystems are connected in parallel with the dc-link capacitors. The first subsystem is comprised of S5, S6, S9, S10, and C2, while the second subsystem is comprised of S7, S8, S11, S12, and C_3. A third subsystem (S1, S2, S3, S4, and C1) is then used to connect the converter to the output phase. In general, an N-level converter can be obtained by cascading (N-1)/2 two-level inverters per subsystem according to Figure 2(b).

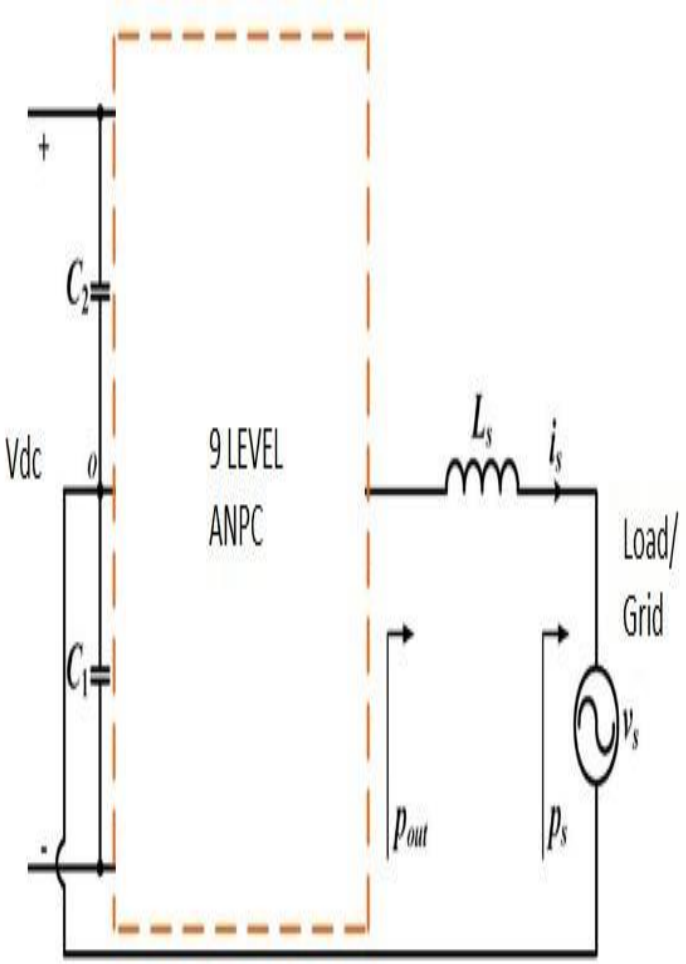


Figure2(a) : Block Diagram

A carrier-based PWM strategy can be used to generate the pulse pattern, as shown in Figure 2(c) [11]. Four triangular carriers are used and phase-shifted by 90°. The first carrier generates pulses to S1 and S2, the second carrier to S3 and S4, the third carrier to S5, S6, S7, and S8, and the fourth carrier to S9, S10, S11, and S12. It is worth mentioning that the switches S5 and S7 are operated in phase, and while S6 and S8 are also in phase, they are complementary to S5 and S7. A similar sequence is applied to S9, S10, S11, and S12. The resulting normalized phase voltage (normalized with respect to half of the dc-link voltage) is also illustrated in Figure 2(c), and it contains nine different voltage levels as shown. For an N-level converter, it would be necessary (N-1) carrier waveforms phase-shifted by 360°/(N-1).

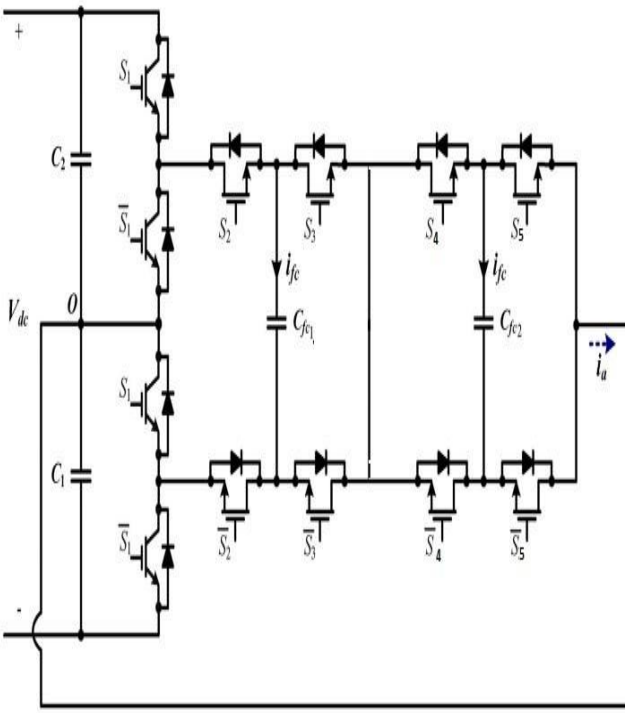


Figure 2(b): Circuit diagram

The voltage blocking capability of the switches in the proposed converter is only U/2, where U is half of the dc link voltage. A generalized converter with N levels would result in a voltage stress across the switches of U/((N-1)/2). It is worth mentioning that a capacitor may be connected between points p and q. Nevertheless, whenever any of the dc- link capacitors is switched in parallel with a capacitor connected between p and q, a loop current would be allowed to circulate in order to balance the voltages across the capacitors being connected in parallel, which might be any of the dc-link capacitors and the capacitor connected between p and q. Such approach is not advantageous for high power applications because the loop current that is created produces losses that are inversely proportional to the carrier frequency and the capacitance value connected between p and q [12].

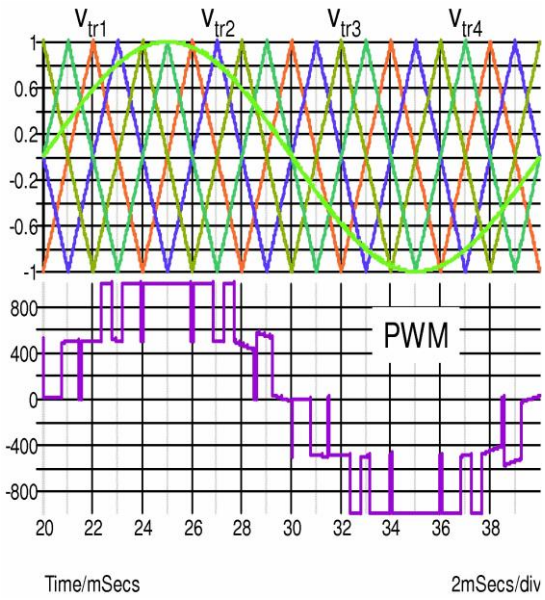


Figure 2(c): Carrier-based PWM and normalized phase voltage

Figure 2(d) shows the normalized voltages (also normalized with respect to half of the dc-link voltage) across the various floating capacitors. As can be seen, natural voltage balancing is achieved using the modulation pattern shown in Figure 2(c). At light load, however, it may be required the connection of booster circuits, which are passive networks to improve the voltage balancing performance [5].

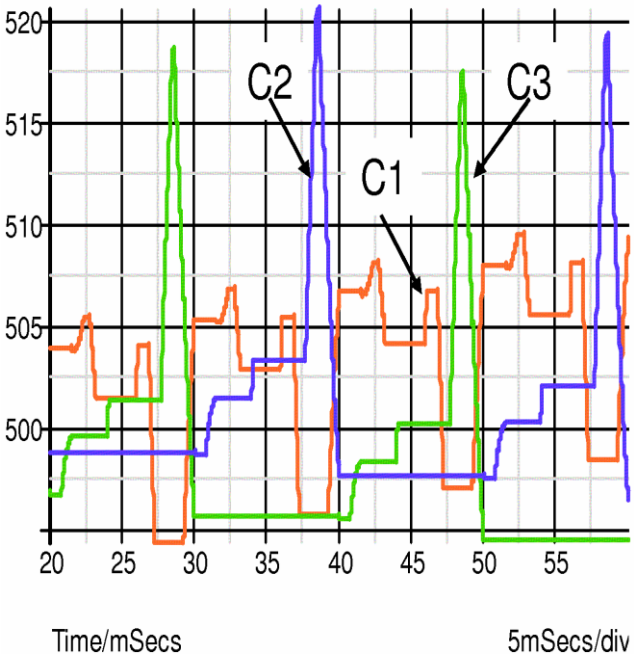


Figure 2(d): Normalized voltage across the floating capacitors

	S1	Sc3	Sc2	Sc1	Output voltage

V1	0	0	0	0	-3vdc
V2	0	0	0	1	-2vdc
V3	0	0	1	0	-2vdc
V4	0	1	0	0	-2vdc
V5	0	0	1	1	-vdc
V6	0	1	0	1	-vdc
V7	0	1	1	0	-vdc
V8	0	1	1	1	-(0)
V9	1	0	0	0	+(0)
V10	1	0	0	1	+vdc
V11	1	0	1	0	+vdc
V12	1	1	0	0	+vdc
V13	1	0	1	1	+2vdc
V14	1	1	0	1	+2vdc
V15	1	1	1	0	+2vdc
V16	1	1	1	1	+3vdc

In some applications, because of the limitations of the size of the dc-link capacitors, the dc link could experience volt- age variations. For example, in single-phase grid-connected applications, the dc-link power can have second harmonic ripple that will cause second harmonic ripple across the dc-link capacitor voltage. In addition, dc-link voltage variations could be caused by applications where an ac rectifier is used to provide the dc-link voltage for the converters.

Generally, the dc-link voltage can have voltage variations in steady-state, dynamic, and transient conditions. In these conditions, capacitor voltages will not be symmetrical. (In this paper, a symmetrical condition is defined as $V_{C1} = V_{C2} = 2V_{Cf}$.) This will result in V_{ao} having more than five different output voltage levels as illustrated in Table I. Further, the difference between the voltage levels is not equal. In this case, voltage condition, will improve controlling ability of the 9L-ANPCinverter system to be applied in a variety of applications.

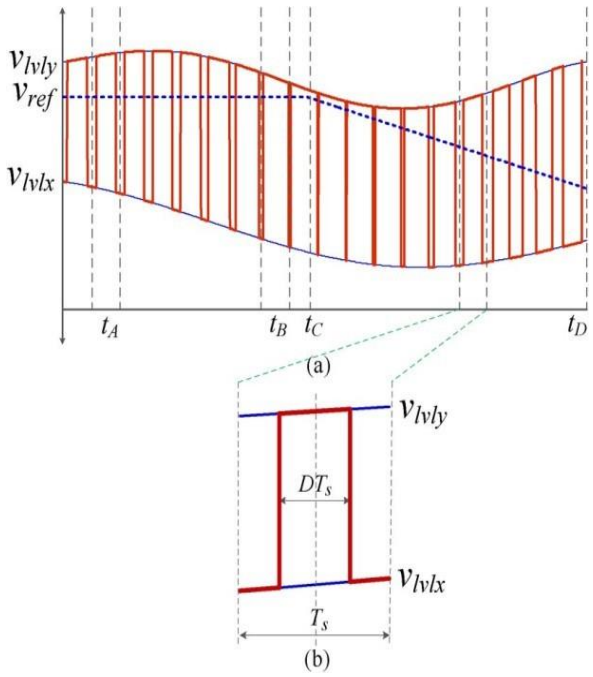


Figure 2(e): Applying variable nearest voltages to generate PWM voltage to track the reference voltage.

In this paper, a novel modulation technique is proposed to determine the appropriate switching states to be selected to generate the requested output voltage and to control the FC voltage to the requested FC voltage during a sampling time both for balanced and unbalanced conditions. Adding FC reference voltage

$$v_{o_s} = \frac{1}{T_s}\int_0^{T_s} v_{\mathrm{ao}}(t)\,dt$$

$$v_{\mathrm{ref}_s} = v_{o_s} = \frac{1}{T_s}\int_0^{T_s} v_{\mathrm{ao}}(t)\,dt$$

$$v_{o_s} = (1 - D_s)v_{\mathrm{lvlx}_s} + D_s v_{\mathrm{lvly}_s}. \qquad (3)$$

Fig. 4 shows the changes in the duty cycle for different operating conditions. For example, to generate the required output voltage during the time periods tA and tB , the duty cycle is varied depending on the chosen voltage levels, vlvlx and vlvly , although in this case, vref is a constant value.

III. Proposed Modulation Technique With FC Voltage Control

In Section II, the operational principles of a five-level FC-based ANPC converter have been discussed for different voltage values across the three capacitors. In the symmetrical condition, the five different voltage levels can be utilized to generate the requested output voltage where some of them have redundancy in the switching state selection. For example, when the output reference voltage is between $V_{dc}/4$ and $V_{dc}/2$, the switching states V_6 and V_8 or V_7 and V_8 can be utilized. To select which of rrent is positive, the selection of V_6 will cause the FC to be discharged; hence, the voltage will be reduced these is to be used (V_6 or V_7), the main objective is to reduce the difference between the reference and the actual FC voltage. Based on (1), to regulate the FC voltage, the polarity of the output current must be considered in selecting the switching states V_6 or V_7. When the polarity of the output cu, whereas the selection of V_7 will cause the FC to be charged; hence, the FC voltage will be increased.

Traditionally, the modulator only requires the output ref- erence voltage as an input, and the FC voltage is assumed regulated to $V_{dc}/4$, and during switching selection in the mod- ulator, the dc-link capacitors are assumed balanced. However, in general, the value of the reference FC voltage has to be taken into account as described in

Section II for balanced and unbalanced dc-link voltages. Therefore, the modulator should have an additional input in the form of the reference FC voltage. This approach provides an improvement to the ability of the modulator and more flexibility for the control system.

Fig. 5(a) shows an operating condition where the capacitor voltages are fluctuating and unbalanced. During the time step T_s shown in Fig. 5(a), seven different voltage levels are available to generate the required output voltage. Based on the averaging technique, the two nearest appropriate voltage levels need to be utilized to generate the requested output voltage. In this case, the voltage level V_{C2} is one of the appropriate nearest voltage levels. Although the voltage level $(V_{C2} - V_{fc})$ is also one of the nearest voltage levels, it may not be the appropriate voltage level to select. A rule to determine the selection of the appropriate voltage level can be based on the effect it has on the FC voltage. For example, during a certain time step, if the actual FC voltage is less than the reference voltage, then the FC must be charged by selecting the appropriate switching state using (1). In (1), if the output current i_a is positive, the selection of the voltage level $(V_{C2} - V_{fc})$ will cause FC to be charged, and if it is negative, the selection of voltage level (V_{fc}) will cause the FC to be charged. Therefore, depending on the sign of (i_a), either the voltage level $(V_{C2} - V_{fc})$ or the voltage level (V_{fc}) need to be selected. The effect of the selection to generate the required output voltage will cause the duty cycle to be varied, as

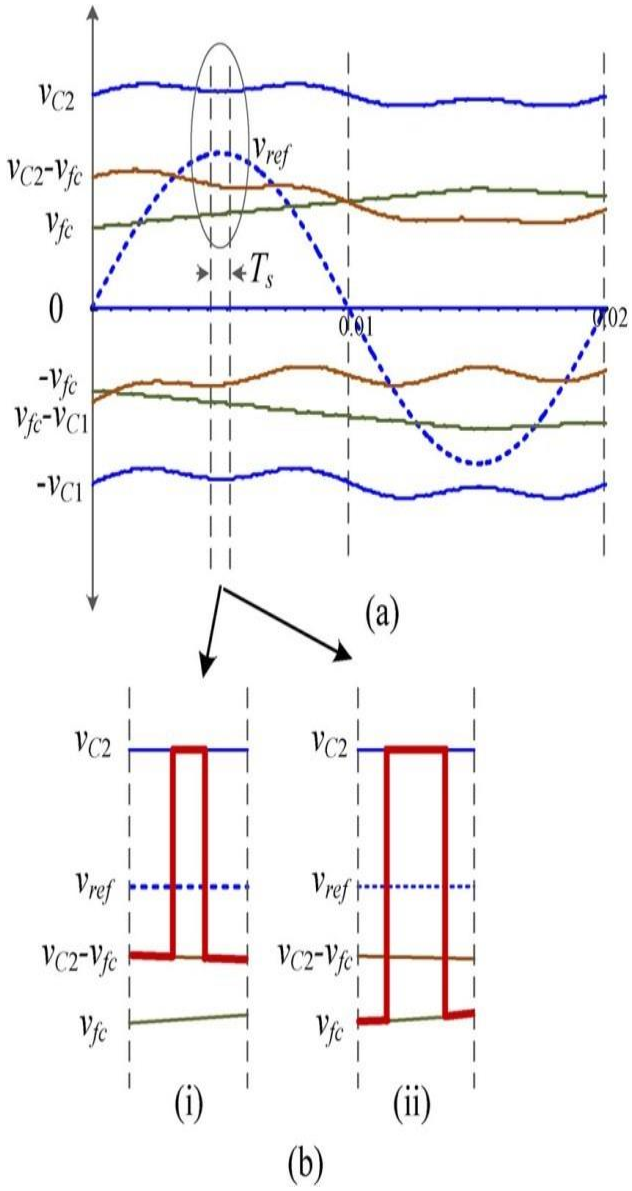


Figure3(a): Applicable voltage levels to implement requested output voltage during a period under varying dc capacitor voltages. 3.(b) Effect of selection of different voltage levels on duty cycle during a special time step to have same reference output voltage.

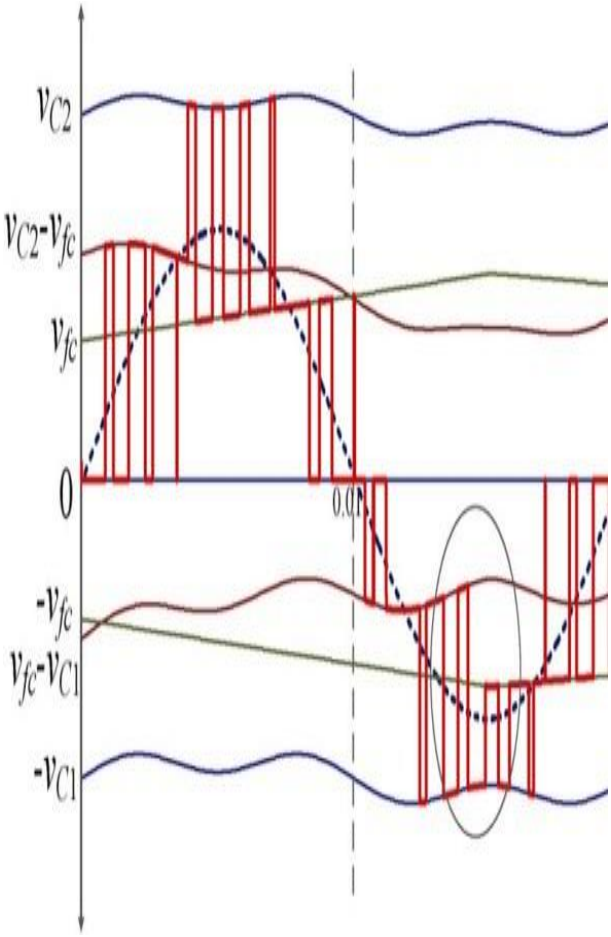


Figure 3(c): Modulator selection of the appropriate voltage level under varying dc capacitor voltages to generate a sinusoidal output voltage.

Fig.3(b). Fig.3(c) shows the modulator selection of the appropriate voltage level under varying dc capacitor voltages to generate a sinusoidal output voltage for a particular reference FC voltage and output current.

Modulator and Control Block Implementation

Fig.3(d) shows the control system diagram consisting of the control block and the modulator. Two systems are compared: one with the conventional modulator, and the other with the proposed modulator. As shown in Fig. 7(b), the proposed mod- ulator can consider unsymmetrical condition in the capacitor voltages to generate the requested output voltage. In this case, the FC voltage can be decoupled from the output voltage, and

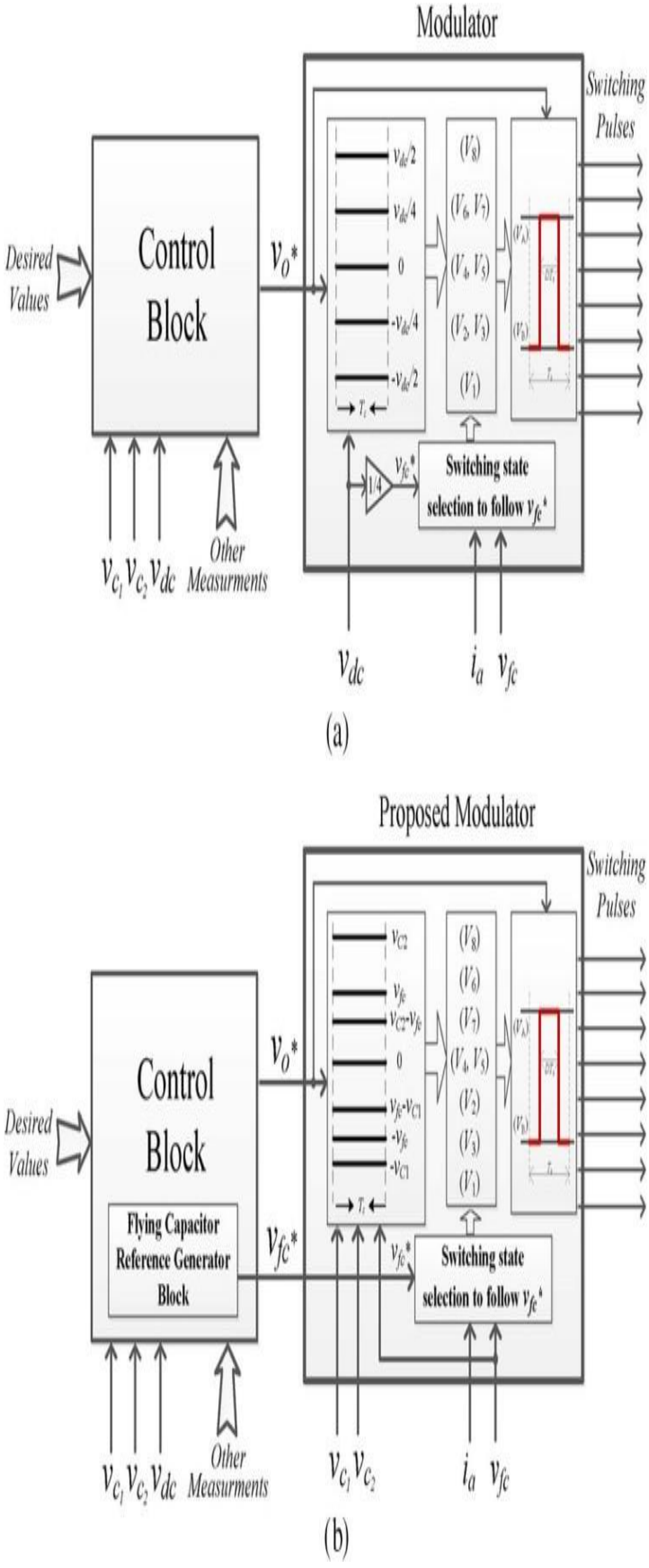


Figure 3(d): Control system diagram then the modulator can accept a new input reference value for FC voltage.

Using FC reference voltage as an input of modulator adds an additional freedom to control the system and the inverter ac side power is in the conventional methods, the control block can only produce and change the requested output voltage of the converter, and the FC voltage is regulated to $V_{dc}/4$. This new dc-link capacitor voltages of the converter in a single-phase application and will be further discussed in the succeeding section.

IV. SINGLE PHASE GRID CONNECTED 9L– ANPC AND PV SYSTEM

A single-phase grid-connected PV system using a 5L-ANPC inverter has the advantage of having high-quality output voltages by using an optimal number of low-voltage switches. One of the important issues in single-phase application is the dc-link capacitor voltage ripple and balancing. In a three-phase three-wire application, the dc-link capacitor voltage balancing can be achieved by controlling the zero-sequence voltage of the inverter. However, in the single-phase structure, because of effect on the output voltage, this technique is not applicable and in this case, the control of the FC voltage can play an important role in solving the problem.

Based on (7) and (8), the power transmitted to the grid and power transferred from the ac side of the inverter have the same dc value but different ac value. To investigate the operation requirements of the modulator and the control system, the dissipation of the inverter is assumed neglected, and the PV modules and the maximum power point tracker (MPPT) circuit are assumed to transfer dc power to the dc side of the inverter, where the value is dependent on the PV modules and the sun irradiation. Therefore, when the system is in a stable condition, the output power from the PV modules with MPPT circuit P_{PV}, shown in Fig. 8 must be equal to the dc part of p_{out}, which is $V_m I_m/2$. If the inverter dissipation is neglected, the difference between p_{out} and P_{PV} must cause the three capacitors of the inverter C_1, C_2, and C_f to experience power ripple. The power ripple in a capacitor will produce voltage ripple across the capacitors as given in the following:

A. Power and Voltage Ripple in the Capacitors

Fig. 8 shows a single-phase grid-connected PV system using a 5L-ANPC inverter. To analyze the system behavior under steady-state conditions, it is assumed that the inverter operates with unity power factor with a low-current total harmonic

This voltage ripple in the dc voltage of the capacitors in the conventional modulator will cause harmonics in the inverter output voltage. Furthermore, it can cause unexpected behavior on the control system action. One solution to reduce the ripple magnitude of the capacitor voltages is to increase the size of the capacitors. This will result in increased cost, size, and weight of the system. Further, it cannot solve completely the issues related to voltage ripple, and any transient on the capacitor voltages can produce unexpected transient on the output voltage and the system behavior.

Moreover, in the grid-connected single-phase 9L-ANPC system, power ripple will not be shared between the capacitors simultaneously. As shown in Table I, when the output voltage is positive, C_2 is transferring power to the output, and when the output voltage is negative, C_1 is transferring the power; however, during the whole period, both capacitors are involved in receiving power from the PV circuit. Therefore, not only the dc-link capacitors have voltage ripple problems because of their power ripple but also they have different timing in their ripples that can produce instantaneous unbalancing of dc-link voltages. To reduce the effect of the dc voltage ripple on the output waveform, the proposed modulation technique in Section III can be used.

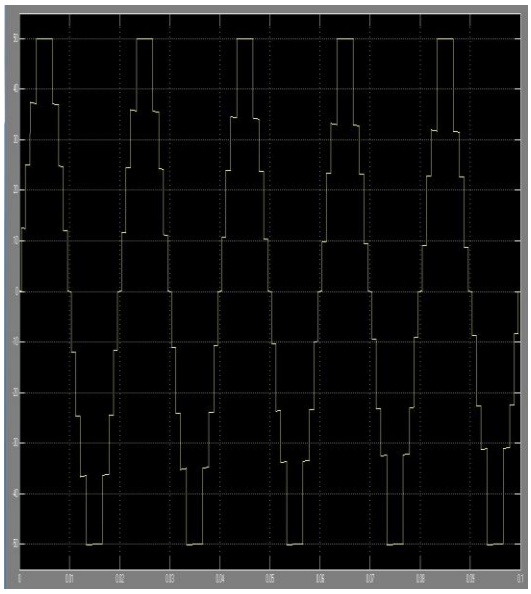
However, two issues still need to be considered: first is the phenoena of the possible divergence of the dc-link capacitor voltages, and second is the selection of the FC voltage reference and its effect on the system.

V. SIMULATION RESULTS

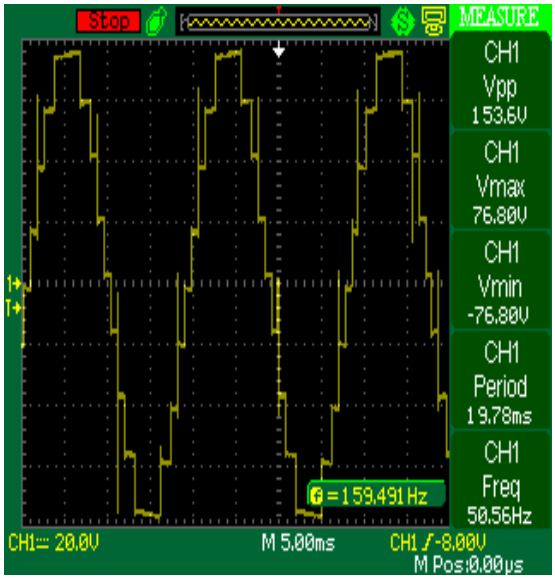
A simulation has been carried out using MATLAB/Simulink to verify the effectiveness of the proposed modulator and control technique for the 9L-ANPC inverter application for a single-phase grid-connected PV system.

VI. EXPERIMENT RESULTS

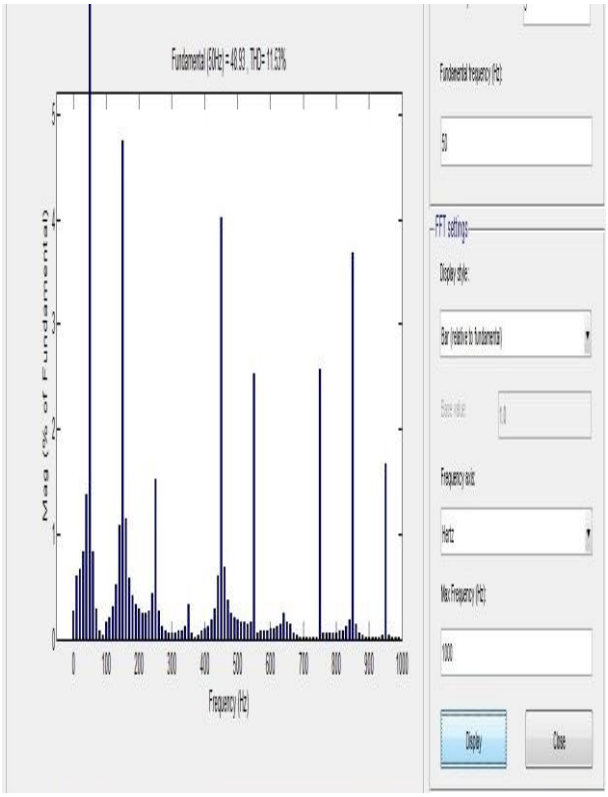
OUTPUT VOLTAGE WAVEFORM:



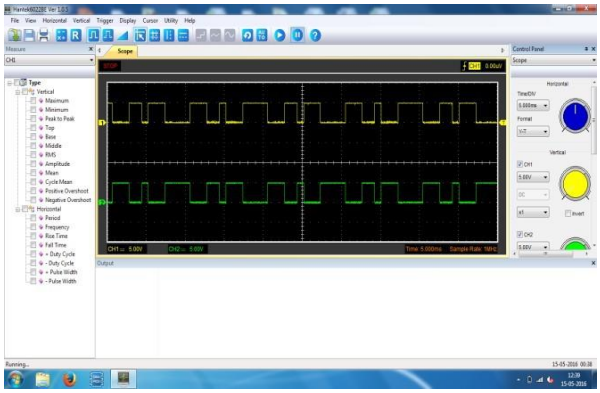
9 LEVEL OUTPUT VOLTAGE:

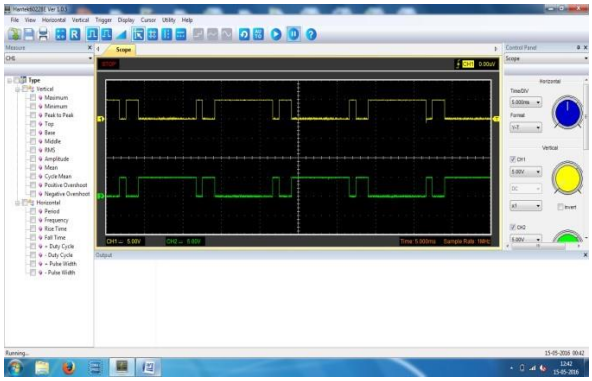


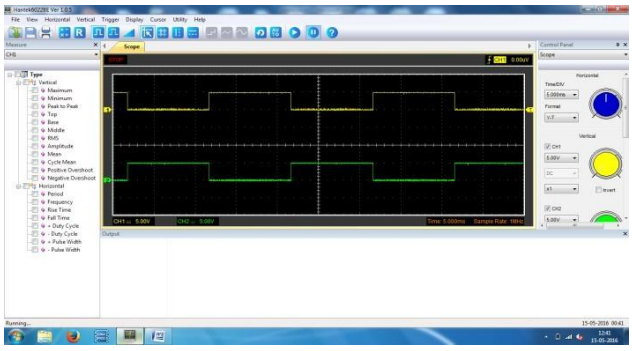
THD:



OUTPUT VOLTAGES FOR DIFFERENT LEVELS:







VDC/2=38V

VII. Conclusion

A theoretical framework of a novel extended modulation technique for unsymmetrical and symmetrical voltage conditions of a 9L-ANPC converter has been proposed. The application of the proposed modulation and control strategy, for a single- phase grid-connected PV system using a nine-level FC-based ANPC converter to produce ac output voltages with good power quality under both symmetrical and unsymmetrical conditions, has been investigated. Issues related to the balancing of dc-link voltages and its associated problems are discussed, and a new control strategy has been introduced to solve the dc-link voltage divergence problem. The proposed strategy is applicable for other applications of the five-level FC-based ANPC converters .In the grid connected system the major problem arises due to power quality issues. These problems under this condition can be removed using the proposed model. The total losses can also be reduced. The proposed system can be used for low voltage high power applications.

REFERENCES

[1] S. Chen, B. Mulgrew, and P. M. Grant, "A clustering technique for digital communications channel equalization using radial basis function networks," *IEEE Trans. on Neural Networks*, vol. 4, pp. 570-578, July 1993.

[2] J. U. Duncombe, "Infrared navigation—Part I: An assessment of feasibility," *IEEE Trans. Electron Devices*, vol. ED-11, pp. 34-39, Jan. 1959.

[3] C. Y. Lin, M. Wu, J. A. Bloom, I. J. Cox, and M. Miller, "Rotation, scale, and translation resilient public watermarking for images," *IEEE Trans. Image Process.*, vol. 10, no. 5, pp. 767-782, May 2001.

[4] P.Barbosa *et al.*, "Active neutral-point-clamped multilevel converters," in *Proc. 36th IEEE PESC*, 2005, pp. 2296–2301.

[5] S.A.Gonzalez, M.I.Valla, and C.F. Christiansen, "Five-level cascade asymmetric multilevel converter," *IET Power Electron.*, vol. 3, no. 1,pp. 120–128, Jan. 2010.

[6] Y.Kashihara and J.Itoh, "Parameter design of a five-level inverter for PVsystems," in *Proc. 8th IEEE ICPE ECCE*, 2011, pp. 1886–1893.

[7] J. Meili, S. Ponnaluri, L. Serpa, P. K. Steimer, and J. W. Kolar, "Optimized pulse patterns for the 5-level ANPC converter for high speed high power applications," in *Proc. 32nd IEEE IECON*, 2006,pp. 2587–2592.

[8] S. R. Pulikanti and V. G. Agelidis, "Control of neutral point and flying capacitor voltages in five-level SHE-

PWM controlled ANPC converter," in *Proc. 4th ICIEA*, 2009, pp. 172–177.

[9] S.R.Pulikanti and V.G.Agelidis, "Hybrid flying-capacitor-based active neutral- point-clamped multi-level converter operated with SHE-PWM," *IEEE Trans. Ind. Electron.*, vol. 58, no. 10, pp. 4643–4653, Oct. 2011.

[10] F. Kieferndorf *et al.*, "A new medium voltage drive system based on ANPC-9L technology," in *Proc. IEEE ICIT*, 2010, pp. 643–649.

[11] T. Geyer, G. Papafotiou, and M. Morari, "Model predictive direct torque control; Part I: Concept, algorithm, and analysis," *IEEE Trans. Ind. Electron.*, vol. 56, no. 6, pp. 1894–1905, Jun. 2009.

[12] L. A. Serpa, P. M. Barbosa, P. K. Steimer, and J. W. Kolar, "Five-levelvirtual-flux direct power control for the active neutral-point clamped multilevel inverter," in *Proc. IEEE PESC*, 2008, pp. 1668–1674.

[13] G. Tan, Q. Deng, and Z. Liu, "An optimized SVPWM strategy for multi level active NPC (9L-ANPC) converter," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 386–395, Jan. 2014.

[14] K. Wang, Z. Zheng, Y. Li, K. Liu, and J. Shang, "Neutral-point potential balancing of a five-level active neutral-point-clamped inverter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1907, 1918, May 2013.

[15] K. Wang, L. Xu, Z. Zheng, and Y. Li, "Capacitor voltage balancing of 5L-ANPC converter using phase-shifted PWM," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1147–1156, Mar. 2015.

[16] Hamid R.Teymour, *Student Member, IEEE*, Danny Sutanto Kashem M. Muttaqi, *Senior Member, IEEE*, and P. Ciufo, Senior Member, IEEE"transactions on industry applications", vol.51,no.2 march/april 2015.