ISSN (ONLINE): 2395-695X
ISSN (PRINT): 2395-695X

International Journal of Advanced Research in Basic Engineering Sciences and Technology (IJARBEST)
Vol. 3, Issue 1, January 2017

This work by IJARBEST is licensed under Creative Commons Attribution 4.0 International License. Available at https://www.ijarbest.com/Archive

High Performance FIR Filter Design using Ancient Indian Vedic Mathematics

Leonard Gibson Moses S[1], Ganesan S[2], Vimala C[3]
Research Scholar/ECE, Periyar Maniammai University, Thanjavur[1]
&
Assistant Professor/ECE, JeiMathaajee College of Engineering, Kancheepuram[1]
Professor/ECE, Mailam Engineering College, Mailam[2]
Professor/Mathematics, Periyar Maniammai University, Thanjavur[3]

***Abstract* -The design of FIR filter is very important for so many DSP applications. So there is requirement of low power and high speed FIR filter. This article presents how the Vedic sutra of Urdhvatiryagbhyam speeds up the computations in FIR filter and reduce the power and layout area. Simulation is performed with ModelSim 6.4a and performance parameters are measured using Quartus II software.**

***Index Terms* - FIR filter, Multiplier and Accumulate unit, Urdhvatiryagbhyam Sutra, Vedic multiplier.**

I. Introduction

In digital signal processing, Impulse response has finite duration in Finite Impulse Response (FIR) filter. The impulse response of Nth order discrete time FIR filters may be continuous time or discrete time, analog or digital.

Vedic mathematics is an ancient mathematics which contains 16 sutras. It deals with various fields in mathematics like algebra, arithmetic and geometry etc., It optimizes the conventional mathematical algorithms. [1]

Multiplication is the operation which takes too much time in mathematical calculations. We can optimize the digital signal processor by optimizing the Multiplier and Accumulate Unit (MAC). By going through the papers [2,3], we can understand the techniques in ancient mathematics thoroughly.

II. Vedic Multiplier

Most of the DSP algorithms use multiplication operation. So, there is a need of high efficiency multiplier. Urdhvatiryagbhyam means vertically and crosswise [4]. It uses a formula which can be applicable to all multiplication cases.

Let us illustrate the multiplication of two decimal numbers as follows:

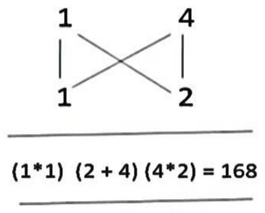


Fig. 1 Multiplication of two decimal numbers - Illustration

Steps:

1. Multiply MSB (1) of first decimal number and MSB (1) of second decimal number. So MSB of answer is 1(1x1=1)

2. Then multiply MSB(1) of first decimal number and LSB(2) of second decimal number; multiply LSB(4) of first decimal number and MSB(1) of second decimal number. So, middle bit of result is the sum of two multiplication results. ((1x2) + (4x1) =6)

3. Finally LSB of result is the result of multiplication of two LSB's of two decimal numbers. (4x2=8)

Using this multiplier, partial product generation is done in parallel and summation also. Due to parallel calculation, this multiplier is not dependent on processor clock frequency.

We know that processing power is directly proportional to clock frequency. Thereby reduce the power consumption a lot. This multiplier can be designed for all NxN bit binary numbers. [5]

III. FIR FILTER

In time domain, the input-output relationship of FIR filter is given by

$$y[n] = \sum_{k=0}^{N} h[k]x[n - k] \quad (1)$$

For N=4, it is given by

$$y[n]=h[0]x[n]+h[1]x[n-1]+h[2]x[n-2]+h[4]x[n-4]$$

Where x[n] represents filter input, y[n] represents filter output, N represents order of the filter and h[k] represents filter coefficients that is nothing but sample response. The output y of a FIR system is calculated by convolving the input signal x with sample response h.

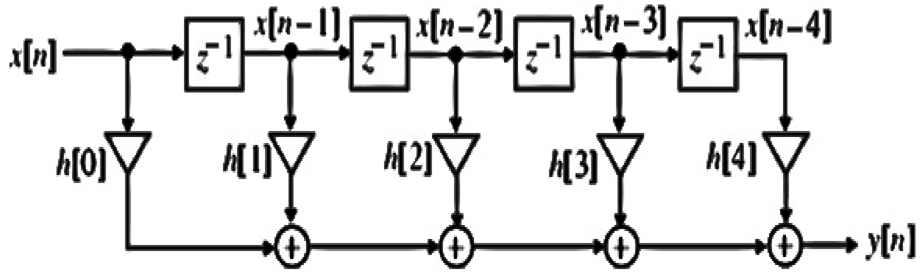


Fig. 2 Direct form of FIR filter

The transpose form of direct form structure is given by

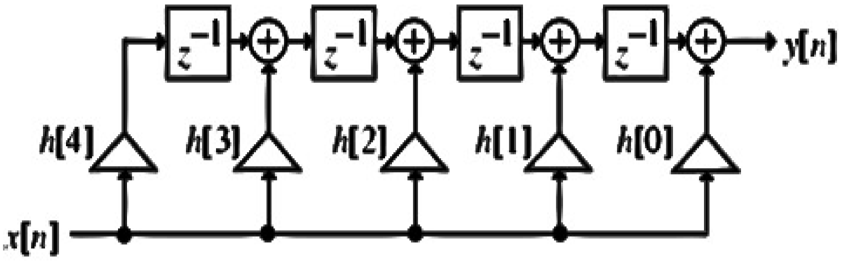


Fig. 3 Transposed form of FIR filter

In direct form, there are delay units between multipliers. At a time, the present filter input, x(n), and N-1 previous samples of the input are fed to each multiplier, and the filter output y(n) is the sum of product of every multiplier. But in transposed form, delay units are between the adders so that the multipliers can be fed simultaneously. For the computation of FIR filter, we have to convolve the input data with filter coefficients.

IV. URDHAVA MULTIPLIER IN MAC UNIT

Multiply – Accumulate unit multiplies the two numbers and sum with accumulator. It has an essential role in computation, especially in digital signal processing. Fig.3 shows the architecture of MAC unit.

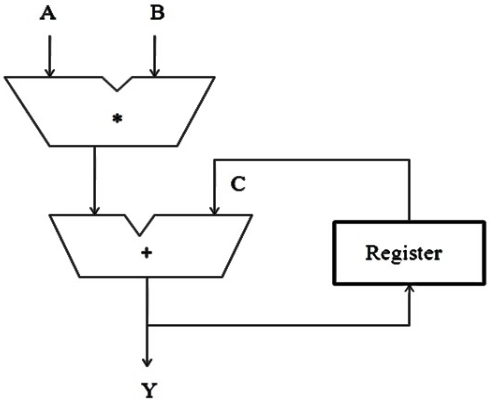


Fig. 4 Hardware architecture of general MAC unit

Here we have designed MAC unit with Urdhva multiplier .The advantages of Vedic multiplier are increasing the speed of computation, decreasing the delay, reducing the power consumption and decreasing the occupied area.

For binary number system, urdhvatiryagbhyam method is given in Fig. 4.

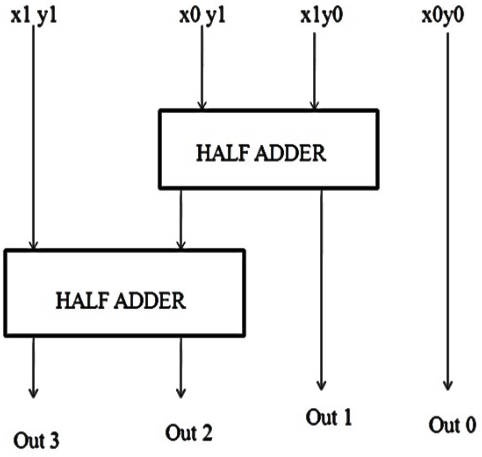


Fig. 5 2x2 binary Urdhva multiplier

The proposed 2X2 Urdhva multiplier is designed by using two half-adders & four 2-input AND gates which is shown in Fig. 4.

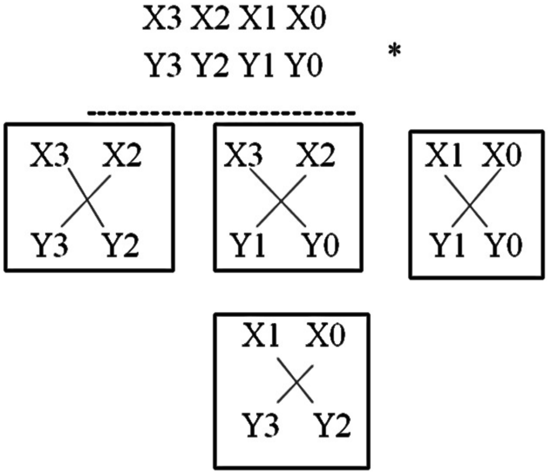


Fig. 6 4x4 binary Urdhva multiplier

The proposed 4x4 Urdhva multiplier module is designed using four 2x2 urdhva multiplier by method of component instantiation which is given in Fig. 5.

Let us assume each multiplication output as,

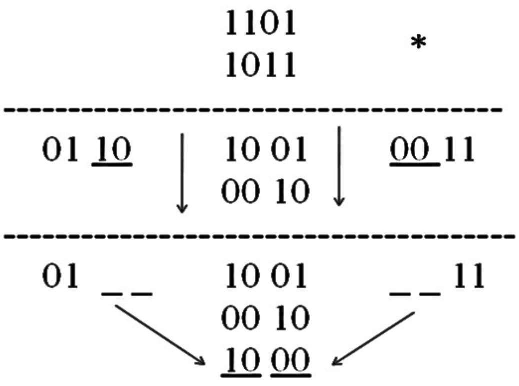


Fig. 7 Multiplication logic using Urdhva method

Fig. 6.shows the multiplication of two 4-bit binary numbers, say 1101(13 in decimal) and 1011(11 in decimal), using the above logic.

First full adder performs addition of 1001 and 0010 giving 1011 as result with no carry. The second full adder performs addition of 1000 with the result of first full adder i.e sum of 1011 and 1000 gives result as 0011 and 1 as carry out. Carry out from first and second full adders is provided to half adder.

Here carryout is generated from second full adder, there by half adder produces 1 as Sum and 0 as carry out. Half adder's sum and carry is then added with S32 (1) and S33 (0) respectively, so Final answer is 10001111 (143 in decimal).

X3X2	X3X2	X1X0	X1X0
Y3Y2	Y1Y0	Y3Y2	Y1Y0
$S_{33}S_{32}S_{31}S_{30}$	$S_{23}S_{22}S_{21}S_{20}$	$S_{13}S_{12}S_{11}S_{10}$	$S_{03}S_{02}S_{01}S_{00}$

Fig. 8 Full adder Illustration

V. RESULTS

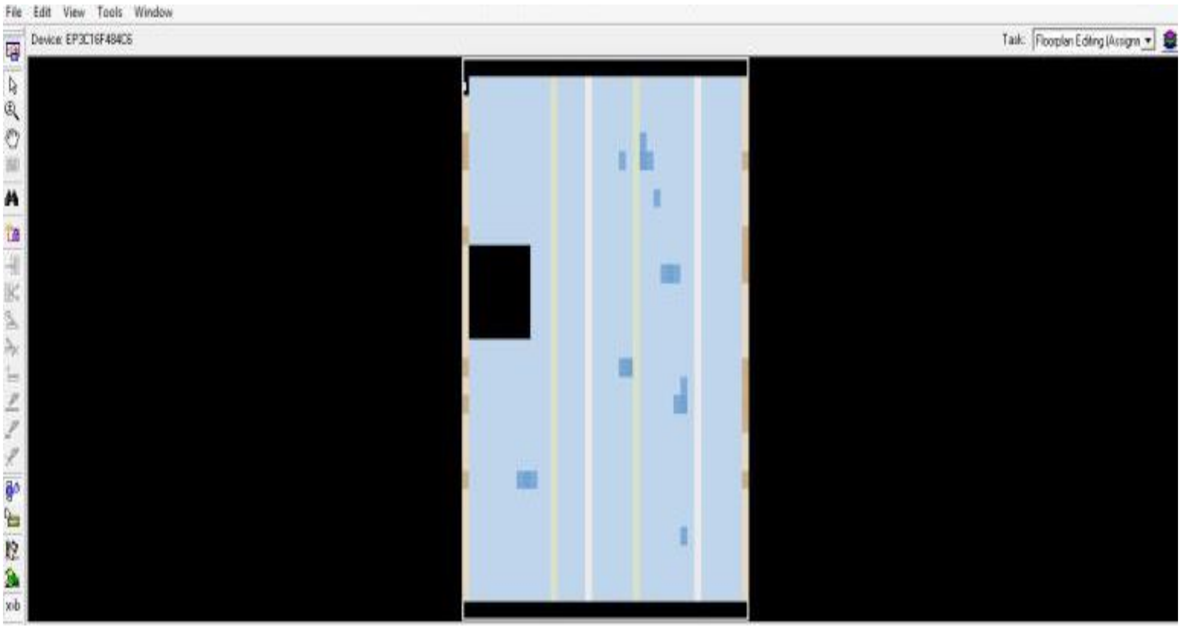
Vedic sutra consumes less number of logical elements so power consumption is reduced as well as layout area is reduced. Computation speed is increased. Table 1.shows the power consumption of FIR Filter using Urdhva method.

TABLE I: POWER CONSUMPTION OF FIR FILTER USING URDHVA

Parameters	Vedic Method
Total Thermal Power Dissipation	68.98mW
Core Static Thermal Power Dissipation	51.74mW
I/O Thermal Power Dissipation	18.23mW

We have used ModelSim 6.4a for simulation of FIR Filter. Power analysis is done using Quartus II 9.0 using EP3C16U484C6 device from the family of Cyclone III.

The Chip planner view of FIR filter design is shown in Fig.7.



Device: EP3C16F484C6

Task: Floorplan Editing (Assign

Fig. 9 Chip planner view of FIR Filter

The technology map viewer- post mapping of FIR filter is shown in Fig.8

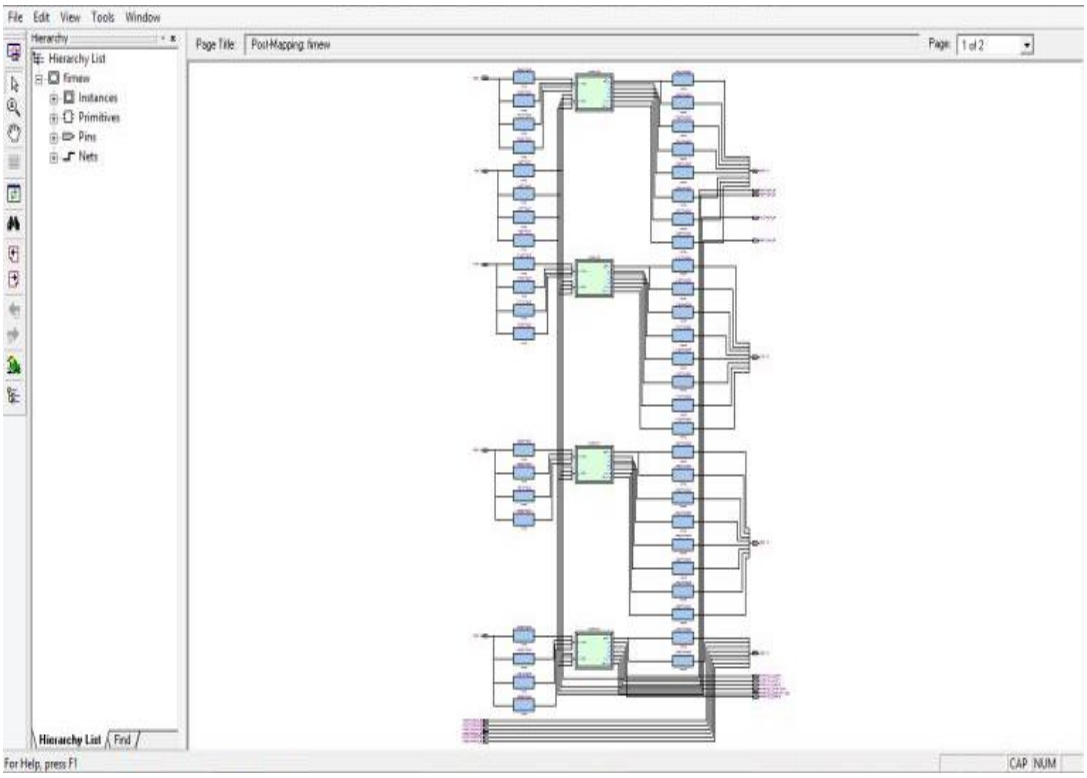


Fig. 10 Technology map viewer-post mapping of FIR Filter

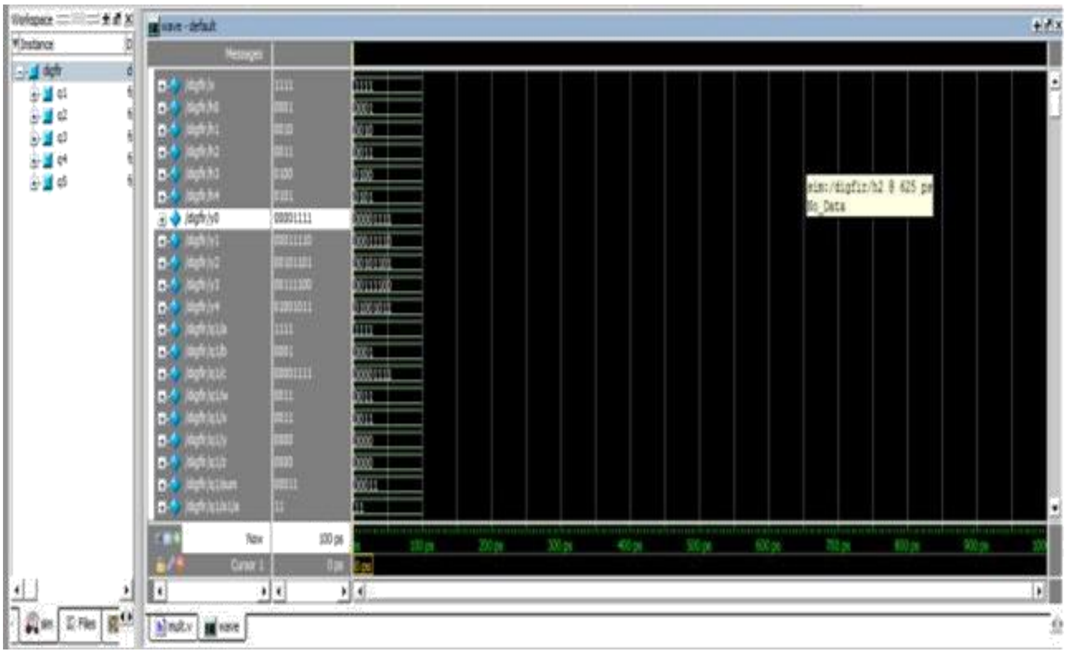


Fig. 11 Simulation result of FIR filter.

VI. CONCLUSION

Thus an efficient multiplier using a Vedic algorithm which has high speed, less complexity and consuming much less area is designed. By using this Vedic multiplier, high performance FIR filter is designed.

REFERENCES

[1] Jagadguru Swami Sri Bharati Krishna Tirthji Maharaja, "Vedic Mathematics", MotilalBanarsidas, Varanasi, India, 1986.

[2] S.G.Dani, "Vedic Maths, Facts and myths", One India One people. Vol 4/6, pp.20-21, 2001.

[3] HimanshuThapliyal, "Vedic Mathematics for Faster mental Calculations and High Speed VLSI Arithmetic", Invited talk at IEEE Computer Society Student Chapter, University of South Florida, 2008.

[4] R.PMeenaakshiSundari and Subathra, "Enhancing multiplier speed in fast Fourier transform based on vedic mathematics", International Journal of VLSIdesign and Communication Systems, Vol.4, No.3, 2013.

[5] M. Poornima, Shivaraj Kumar Patil, ShivuKumar, K.P.Shridhar, and H.Sanjay, "Implementation of Multiplier algorithm using Vedic Mathematics", International Journal of Innovative Technology and Exploring Engineering, Vol.2, Issue 6, 2013.