ISSN (ONLINE): 2456-5717
International Journal of Advanced Research in Basic Engineering Sciences and Technology (IJARBEST)
Vol.3, Issue.11, November 2017

Design and Implementation of Five Level Multilevel Inverter Fed Motor Drive

N.Priya[1], P.Narasimman[2]
[1, 2] Assistant Professor, Department of Electrical & Electronics Engineering,
Kings College of Engineering, Thanjavur, India

Abstract— **In recent years, multilevel power converters have been receiving increased attention because they can withstand high voltage and engender a proximately sinusoidal waveform. Large-motor drive systems are generally utilized with transformers to control the voltage stress on semiconductor devices in the converter circuit. If multilevel converters are instead used for this purpose, the transformers can be omitted because these converters reduce the voltage stress on each switching device. However, multilevel converters have certain disadvantages such as the need to balance the voltage of the dc-bus capacitors. In this paper a novel five level diode clamped multilevel inverter is proposed. A three phase five level diode clamped multilevel inverter is analyzed through simulation using MATLAB® Simulink and it is implemented in hardware. The Total Harmonic Distortion (THD) of five level diode clamped multilevel inverter (DCMLI) is verified and the results are compared.**

Index Terms—**Diode clamped multilevel inverter (DCMLI), Total Harmonic Distortion (THD).**

I. INTRODUCTION

Power-electronic inverters are becoming more popular for various industrial applications. In recent years high-power and medium-voltage drive applications have been installed [1]. To overcome the limited semiconductor voltage and current ratings, some kind of series and/or parallel connection will be necessary. Due to their ability to synthesize waveforms with a better harmonic spectrum and attain higher voltages, multi-level inverters are receiving increasing attention in the past few years [9],[10].

The multilevel inverter was introduced as a solution to increase the converter operating voltage above the voltage limits of classical semiconductors. The multilevel voltage source inverter is recently applied in many industrial applications such as AC power supplies, static VAR compensators, drive systems, etc. One of the significant advantages of multilevel configuration is the harmonic reduction in the output waveform without increasing switching frequency or decreasing the inverter power output. The output voltage waveform of a multilevel inverter is composed of the number of levels of voltages, typically obtained from capacitor voltage sources. The so called multilevel starts from three levels. As the number of levels reach infinity, the output THD (Total Harmonic Distortion) approaches zero [3], [9]. The number of the achievable voltage levels, however, is limited by voltage unbalance problems, voltage clamping requirement, circuit layout and packaging constraints. Multilevel inverters synthesizing

a large number of levels have a lot of merits such as improved output waveform, a smaller filter size, a lower EMI (Electro Magnetic Interference) and other advantages [2].

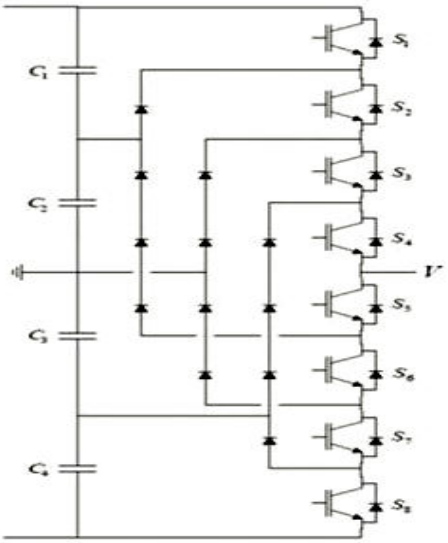

Fig 1. Five level diode clamped multilevel inverter.

II. DIODE CLAMPED MULTILEVEL INVERTER [DCMLI]

One of the multilevel structures that has gained much attention and widely used is the Neutral-Point-Clamped multilevel inverter or also known as Diode Clamped multilevel inverter [4][5]. DCMLI multilevel inverters synthesize the small step of staircase output voltage from several levels of DC capacitor voltages. An m-level DCMLI inverter consists of (m-1) capacitors on the DC bus, 2(m-1) switching devices per phase and 2(m-2) clamping diodes per phase. Figure 1 shows the structure of 5-level DCMLI.

TABLE I SWITCHING STATES OF 5 LEVEL DCMLI

Power device Index	Output Phase Voltage (V_o)				
	V_1	V_2	V_3	V_4	V_5
S_1	1	0	0	0	0
S_2	1	1	0	0	0
S_3	1	1	1	0	0
S_4	1	1	1	1	0
S_5	0	1	1	1	1
S_6	0	0	1	1	1
S_7	0	0	0	1	1
S_8	0	0	0	0	1

The DC bus voltage is split into 5 levels by using 4 DC capacitors, C1, C2, C3 and C4. Each capacitor has $V_{dc}/4$ volts and each voltage stress will be limited to one capacitor level through clamping diodes [6], [7]. The output voltage, V_o has three states as given in Table 1.

The number of levels can be extended to a higher level by additional switching devices and with these additions, the inverter will be able to achieve higher AC voltage, producing more voltage steps that will be approaching sinusoidal with minimum harmonics distortion. During inverter operations, the switches near the centre tap are switched on for a longer period compared to the switches further away from the centre tap as given in the switching states in Table 1. As the switch is further away from the centre tap the switching time is shorter. Another difference between the conventional 2-level and multilevel DCMLI is the clamping diode.

III. MATLAB® SIMULINK MODEL

The 3-phase, 5-level DCMLI multilevel inverter consists of twenty four IGBTs, eighteen clamping diodes and four capacitors as illustrated in Figure 2.

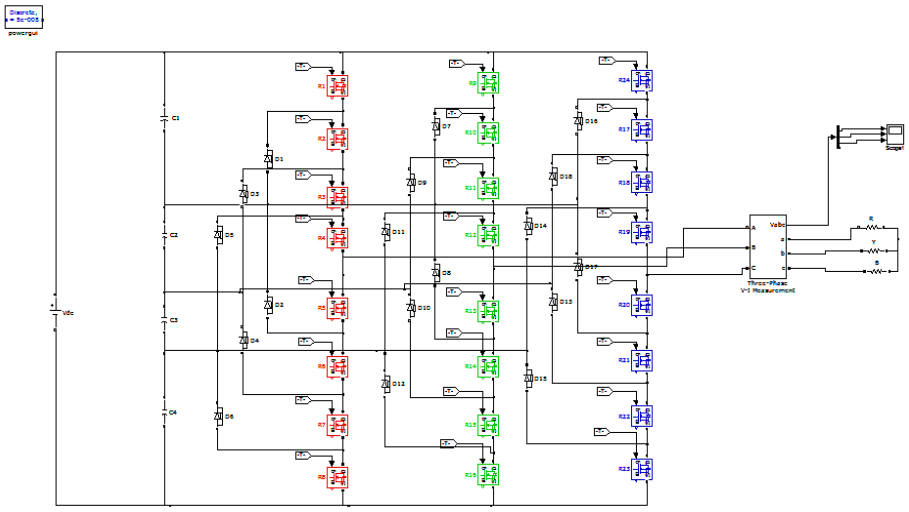

Fig 2. SIMULINK® realization of five level diode clamped multilevel inverter.

The clamping diodes are connected in such a way that it blocks the reverse voltage of the capacitor. four capacitors have been used to divide the DC link voltage into five voltage level i.e. $+V_{dc}$,$+V_{dc}/2$, 0V, $-V_{dc}/2$, $-V_{dc}$. thus the name of 5-level. In this work, twenty four triggering signals are needed for the 5-level DCMLI inverter. These signals should be synchronized with the AC supply voltage. Since the MATLAB® Simulink does not have such triggering block set, a new triggering block has been designed and developed using the block set obtained from Simulink Toolbox. Also, the gate signals sequence and duration of conduction angle of the IGBTs has been determined.

The figures from 3 to 6 are the simulation results of the line voltage and %THD of the three level and five level DCMLI.

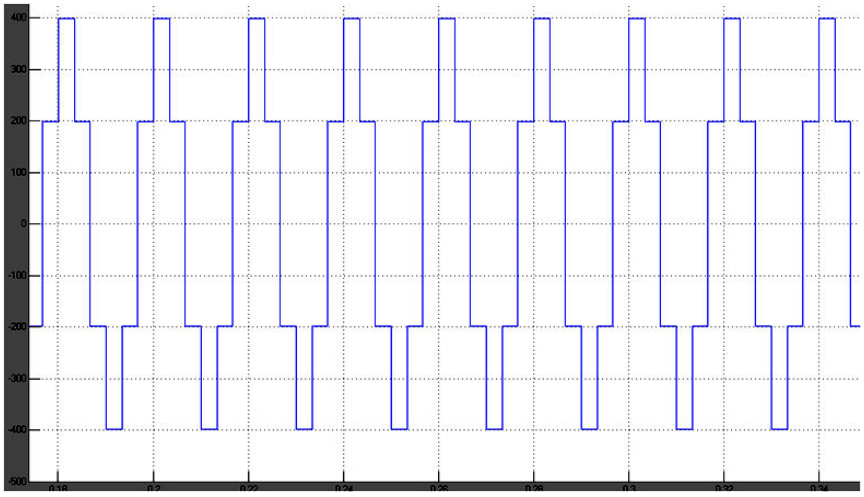

Fig 3. Line to Line voltage of three level DCMLI

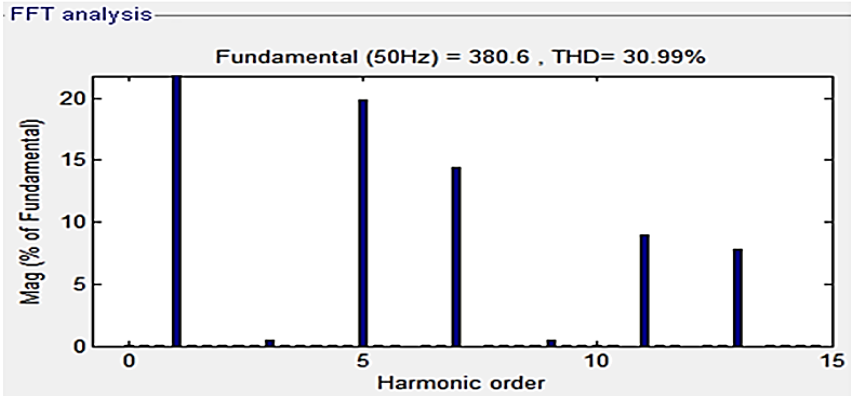

Fig 4. FFT Analysis of three level DCMLI

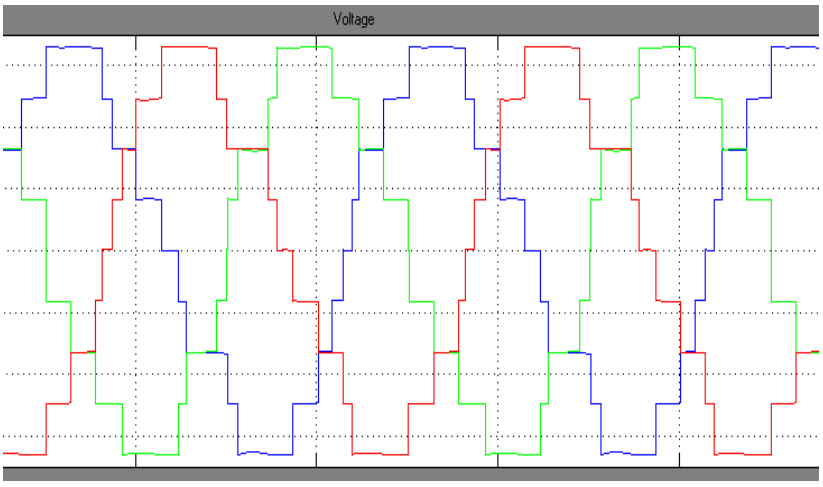

Fig 5. Line to Line voltage of five level DCMLI

Figure 3 shows the line to line voltage of developed 5-level DCMLI inverter with resistive load.

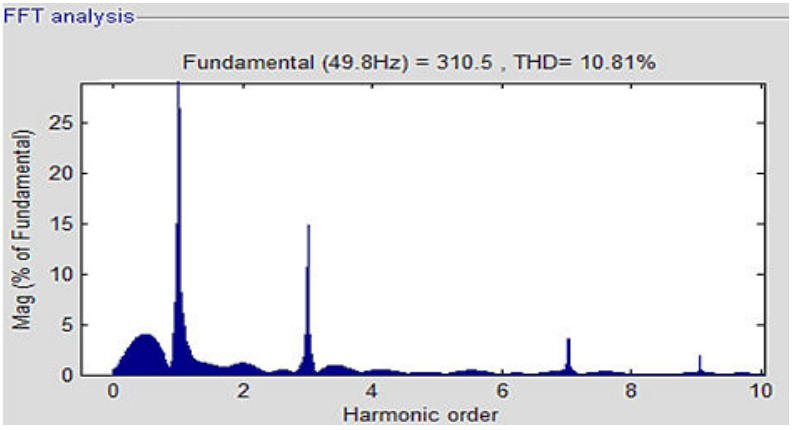

Fig 6. FFT Analysis THD in five level DCMLI

Since %THD of the proposed five level DCMLI is less, the same is implemented in hardware and %THD is analyzed using Power Quality Analyzer (PQA).

IV. HARDWARE SETUP AND RESULTS

The DCMLI inverter needs twenty four gate pulses to trigger the IGBTs. A triggering circuit comprises of AT89C51 microcontroller, MCT2E optocouplers and IR2110 IGBTs drivers have been designed. Figure 7 shows the block diagram of the laboratory model of the proposed five level DCMLI's triggering circuit and phase shift circuit.

AT89C51 microcontroller has been programmed to generate the twenty four pulses for the IGBTs power circuit. As a protection for the microcontroller between the high voltage and low voltage devices, MCT2E optocouplers have been selected as the isolation devices. Single channel IGBTs driver IR2110 has been chosen as the driver to provide the required voltage and power to switch on and off the IGBTs. It also functions as an isolation device.

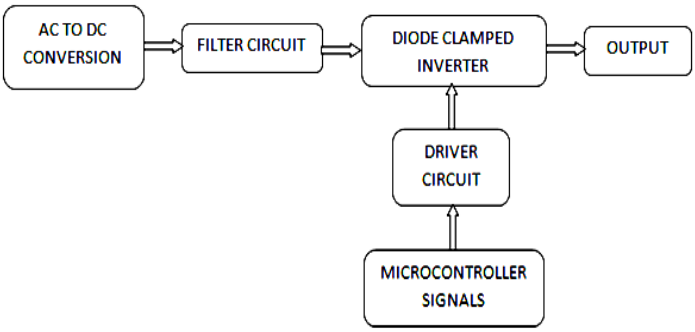

Fig 7. Block diagram of DCMLI

Figure 8 shows the hardware setup of the 5-level DCMLI with power quality analyzer (PQA). Figures 9 and 10 give the measured line to line voltage and harmonic output obtained for the proposed five level DCMLI using Power Quality Analyzer (PQA).

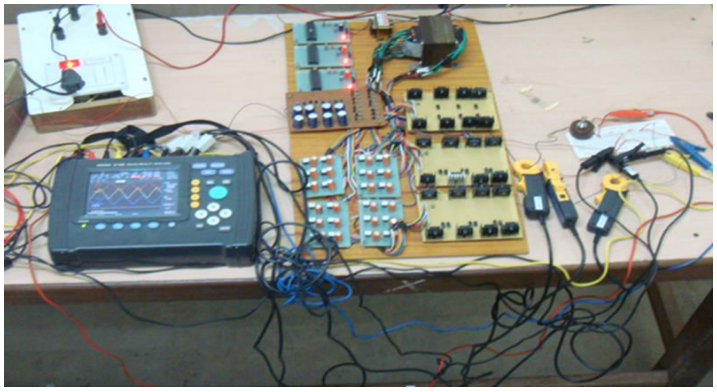

Fig 8. Hardware setup of 5-level DCMLI with Power Quality Analyzer

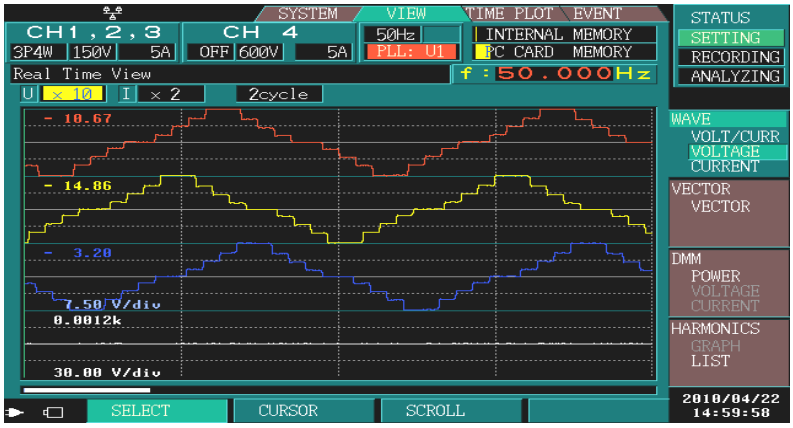

Fig 9. Line to Line voltage waveform of 5-level DCML inverter in Power Quality Analyzer

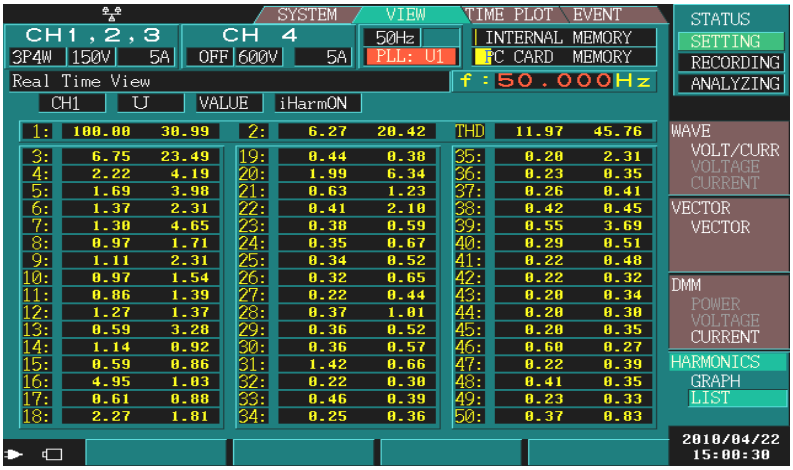

Fig 10. Harmonics order per phase of 5-level DCMLI in Power Quality Analyzer

TABLE II COMPARATIVE RESULTS OF THE THREE AND FIVE LEVEL DCMLI

Simulation		Hardware
Three Level DCMLI	Five level DCMLI	Five level DCMLI
30.99 %	10.81%	14.27%

V. CONCLUSION

The feasibility of the five level DCMLI is made in this paper. From the simulated and experimented results it is concluded that the proposed five level DCMLI has less %THD compared to three level DCMLI and the voltage of the dc-bus capacitors is well balanced. But the reason for variation in experimental %THD over simulation is to be analyzed as a future scope.

REFERENCES

[1] Abhijit Kadam and Anshuman Shukla," A Multilevel Transformer less Inverter Employing Ground Connection Between PV Negative Terminal and Grid Neutral Point" IEEE Transactions on Industrial Electronics ,Volume: 64, Issue: 11, Nov. 2017, pp. 8897 – 8907.
[2] P.Narasimman and E.Latha Mercy, "Design and Comparison of Controller for the Reduction of Conducted Electromagnetic Interference in an Inverter" –Published in Emerging Technology Trends in Circuits and Systems of Circuits and System, Vol. 7, No.7, 2016, pp.1167-1176.
[3] E.Latha Mercy, R Rajesh, Anu Chacko and P.Narasimman," Comparative Analysis of Harmonic Elimination in PV Based Multilevel Inverter Using Ant Colony and Bee Algorithms", Published In International Journal of Applied Engineering Research. Vol: 10 No: 76, 2015, pp. 301- 306.
[4] M. H. Rashid, "Power electronics circuits, devices, and applications, "International: Prentice Hall, 2004.
[5] H. Akagi, H. Fujita, S. Yonetani, and Y. Kondo, "A 6.6-kVtransformerless STATCOM based on a five-level diode Clamped PWM converter: System design and experimentation of a 200-V, 10-kVA laboratory model," Conf. Proc.IEEE-IAS Annu. Meeting, pp. 557-564, 2005.
[6] Z. Pan, F. Z. Peng, K. A. Corzine, V. R. Stefannovic, J. M.Leuthen, and S. Gataric, "Voltage balancing control of diode clamped multilevel rectifier/inverter systems, "IEEE Trans. On Ind. Appl., vol. 41, no. 6, pp.1698-1706, 2005.
[7] J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel inverter: A survey of topologies, control, and applications, "IEEE Trans. Ind. Electronics. vol. 49, no. 4, pp. 724-738, 2002.
[8] C. Newton and M. Sumner, "Novel technique for maintaining balanced internal DC link voltages in diode clamped five-level inverters, "IEE Power Appl., Proceedings, vol. 146, issue 3, pp.341-349, 1999.
[9] S. Malik and D. Kluge, "ACS 1000 world's first standard ac drive for medium-voltage applications" ABB Review, no.2, pp.4-11, 1998.
[10] C. Newton and M. Sumner, "Neutral point control for multilevel inverter: theory, design and operational limitations," Conf. Rec. IEEE-IAS Annu. Meeting, vol. 2, no. 5, pp. 1336-1343, 1997.