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Design of Register Files used in Low Power S-RAM

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Abstract: - This project propose that the design of new static random access memory (SRAM) for low power consumption. The main aim is to design resigter files which is dedicates high bandwidth memory operations as the discharging current continues raising in each and every generation of VLSI processing technology, appropriate selection of the local and global bit-line organization of Register files becomes an important design issue for low power and high performance applications. Memory array cells, sense amplifier and buffer are the essential components of the register files. In this paper register files designs are analysed for various parameters such as for Load Capacitance, Supply voltage and Temperature at different CMOS technologies like 90nm, 65nm and 45nm. The schematic are drawn in DSCH software and the layouts are drawn in MICROWIND software for the analysis.

Keywords: - **Register files, Power Consumption, Bandwidth, and CMOS Technology.**

I. INTRODUCTION

Low power has emerged as a principle theme in electronic industry. The need for low power has caused a major pattern where power dissipation has become an important consideration in area and performance. The need for low power design is motivated by several factors, such as the emergence of portable systems like batteries. The evolution of portable or mobile communication devices such as laptops, cellular phones, personal computing devices and wireless communication systems increase the need for low power applications. Expensive packaging and cooling strategies are required as the chip consumes more power. Hence there will be an added advantage in designing low power application hence it consumes less power. The main reason behind the development of low power circuits are that many portable devices and their applications require low power dissipation and high throughput. Thus low power design of digital integrated circuit is currently a rapid developing field now-a-days.

II. LITERATURE REVIEW

"Characterization of a low leakage current and high speed 7T SRAM circuit with wide voltage margins" by Khawar Sarfraz and Volkan Kursun says that this approach is about the read and write operation of SRAM giving an output of low power consumption of power [1].

"Low Power SRAM Design with Reduced Read/Write Time" by Shivani Yadav, Neha Malik, Ashutosh Gupta and Sachin Rajput says that this paper focuses on the optimization of delay and power [2].

"Memory", Lecture notes for ECEN 6263 by Louis.G. Johnson provides the read and write operation for 10 ports has been discussed in here. [3].

"Static-Noise-Margin Analysis of Modified 6T SRAM Cell during Read Operation" By Nahid Rahman1, Gaurav Dhiman1 and B. P. Singh says about the noise effect of different SRAM

cells and it represents the modified 6TSRAM cell which is used to increase the stability without increasing the transistor count.[4].

Software(s) Used

1. Digital Schematic(DSCH 3)
2. Microwind 3.5

1. DSCH 3

The DSCH (Digital Schematic 3) program is a logic editor and simulator. DSCH is going to be used to examine the structure of the logic circuits before the microelectronics model is started out. DSCH presents a convenient to use environment for hierarchical logic model, and quick simulation with delay research, that enables the design and affirmation of intricate logic circuits .DSCH as well characteristics the logo designs and assembly support for 8051 and 16F84 controllers. Developers can make logic circuits for interfacing with such controllers and confirm software products using DSCH.

2. MICROWIND

MICROWIND software tool is the industry's most comprehensive package dedicated to microelectronics and Nano technology, ASIC and custom IC design and simulation, as well as the latest in electronic and automation design

III. EXISTING METHOD

OPERATIONS

The basic operation of SRAM cells are *Stand-By Mode, Read Mode* and *Write Mode*.

a) Stand-By Mode

In the stand-by mode both transistors PMOS and NMOS are in 'OFF' state and leakage is reduced. WL=0(word line), whatever changes occurs in the bit line (BL), no effect takes place at storage node.

b) Read Mode

WL=1, storage node value based on bit line value i.e. BL AND BL BAR.

c) Write Mode

WL=0,after read mode only write mode have to perform, so storage nodes retain the same data as per read node, but cannot change the value of storage nodes whatever change occurs at bit line. The process of storing a data is known as Write operation and the process of recovering the data is known as Read operation.

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6T Design Using Dsch3

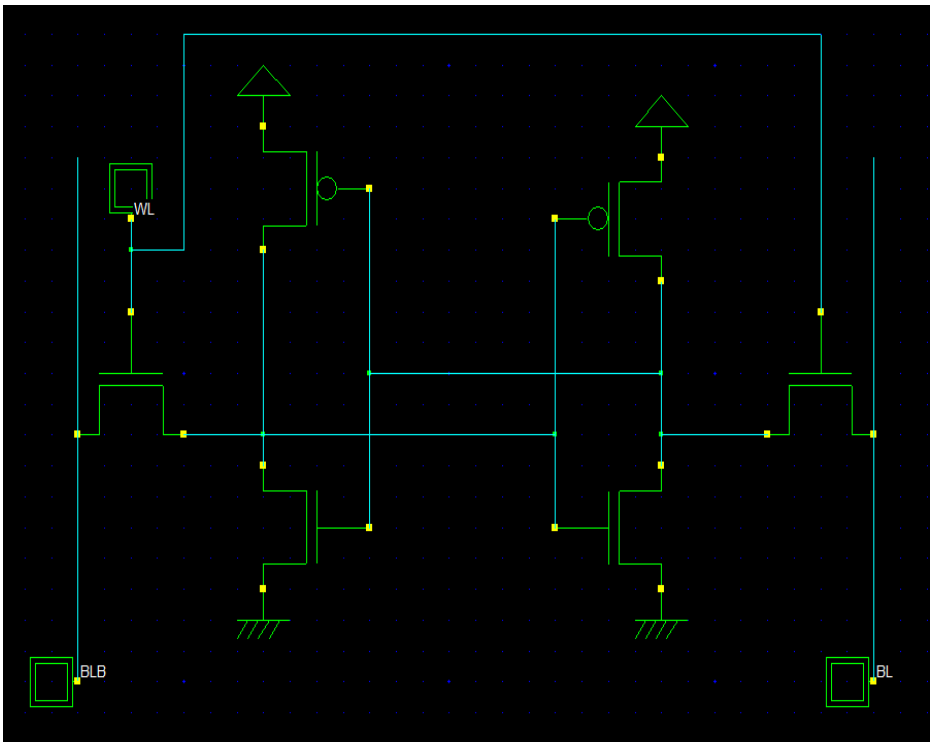

Fig. 1.1 6T design

Here the inputs WL (word line), BL (bit line) and BLB (bit line bar) are represented by means of input switches.

6T Using Microwind Layout

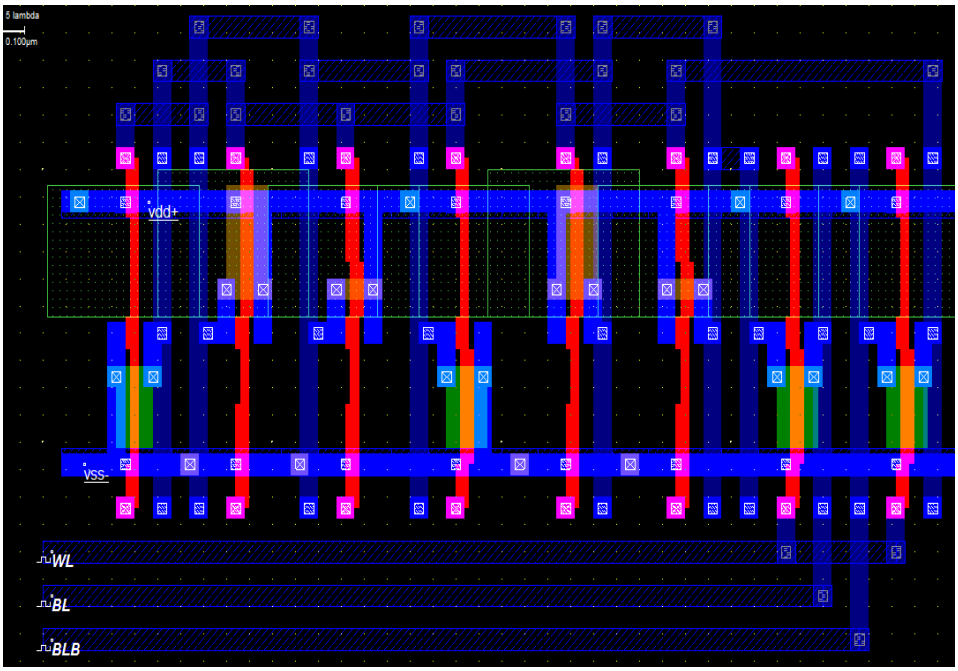

Fig. 1.2 6T using MICROWIND

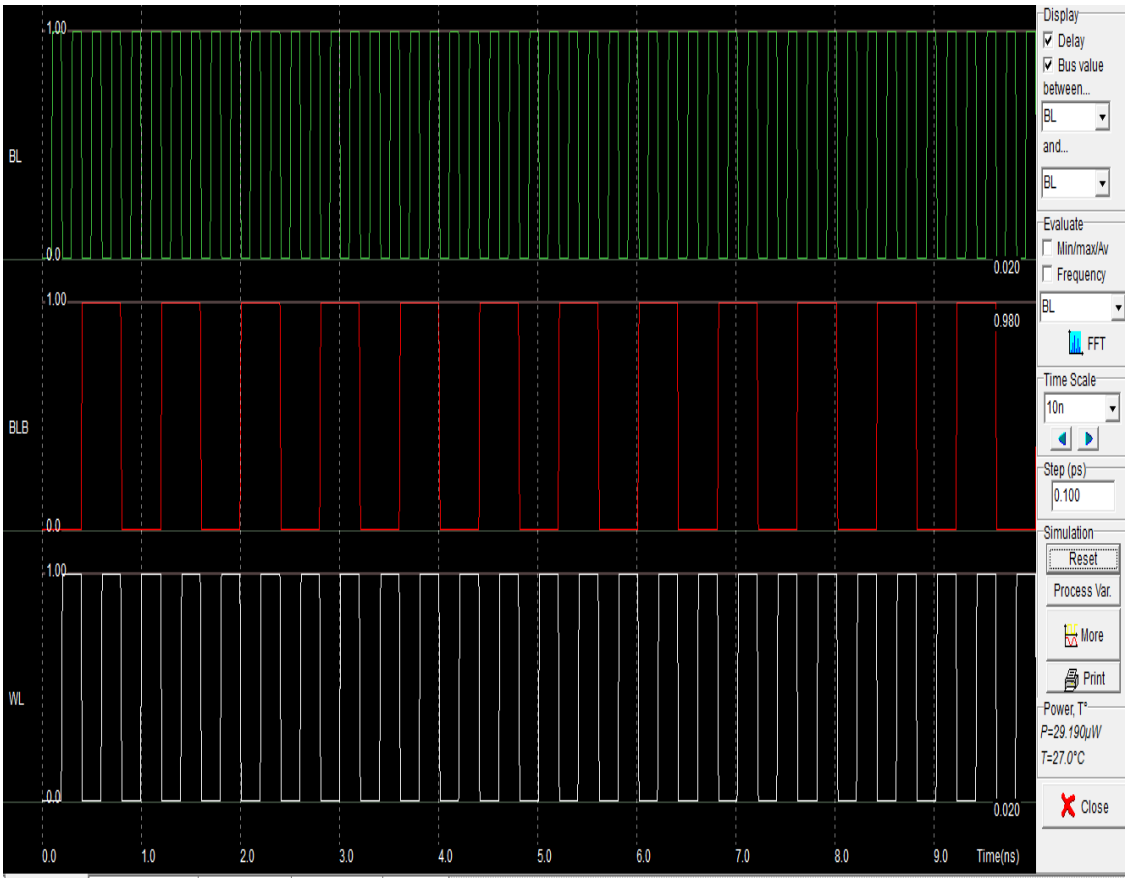

Fig. 1.3 6T using MICROWIND

The above graph indicates that when both the word line and bit line is high the data is written on the memory and the power is calculated as 29.190mw.

7TSRAM Cells

The write performance will begin by switching off the transistor to discontinue the feedback connection. At the time of read operation, the cell act as a conventional 6T SRAM cell. The above circuit reduces the leakage current by adding an extra transistor to the normal 6T circuit that is available in practice. Since the leakage current is reduced it results in reduced power of 0.219mw.

8T S-RAM Cell

This 8T SRAM cell is same as the 7T SRAM cell but it consist of additional two transistors (thus yielding an 8T cell design) are employed in to reduce the leakage current. The additional transistors decreases the leakage current further and the power consumption is only around 33.488microwatt.

10T S-RAM Cell

6T SRAM cell and an additional read circuits are in the 10TSRAM cell. Trouble in conventional 6T SRAM cell is the high data loss during read operations. There is possibility of flipping node voltage at the output due to back to back inverter actions. This situation can be avoided using extra read circuitry.

11TSRAM Cell

The read word line RWL is distinct from the write word line (WL). To store the data at the storage nodes Q and Q', the read word line RWL is set to be low. The switching behavior of the transistors is decided by the voltage at the storage nodes. Since no current flows between storage nodes and bit lines, the read SNM (signal noise margin) is almost equal to ideal hold SNM The write operation in the proposed cell is performed by setting the bit lines (BL and BLB) to the desired logic before asserting WL=Vdd. Here in4 represents the word line (WL), in3 denotes the bit line (BL) and in4 denotes the bit line bar (BLB). The power dissipation analysis for 11t is obtained as 3.290microwatts.

SENSE AMPLIFIER

In modern computer memory, a sense amplifier is one of the elements which make up the circuitry on a semiconductor memory chip (integrated circuit). A sense amplifier is a part of the read circuitry that is used when data is read from the memory, its role is to sense the low power signals from a bit line that represents a data bit (1 or 0) stored in a memory cell, and amplify the small voltage swing to recognizable logic levels so the data can be interpreted properly by logic outside the memory.

TRISTATE BUFFER

A tri-state buffer is a device that allow us to control when current passes through the device, and when it doesn't. A tri-state buffer has two input s: a data input **a** and a control input **c**. The control input acts like a valve. When the control input is dynamic, the output is the input. That is, it act as a normal buffer. The "valve" is exposed. When the control input is not active, the output is "Z". The "valve" is open, and no electrical current flows through. Thus, even if **a** is 0 or 1, that value does not flow through.

IV. PROPOSED METHOD

2X2 6T SRAM ARRAY

The 6T array design has increased write stability, with reduced size and power consumption of a standard 6 transistor SRAM cell. The6T cell symbol is obtained, and the power consumed by the cell is analyzed. The 2x2 array is capable of storing 4 bits of information at a time.
The waveform shows the write operation done on a 6T array and it is observed that the power consumed by the 6T array is found to be 0.159mw.

2X2 7T SRAM ARRAY

It contains of single-ended write operation. In write operation cell needs either differential voltage bias or asymmetrical inverter characteristics. It provides stability to minimize leakage current. An extra transistor is added to the SRAM 6T cell to separate read and write operation, it gives the single-ended 7T SRAM cell array.

2X2 8T ARRAY

An eight-transistor (8T) cell is presented to progress the ability and low-voltage performance with high-speed SRAM caches. The 8T SRAM cell can store 4 bits of data with minimum power requirement.In this array, word lines (WWL and RWL) are shared among cells in one

row and bit lines (WBLs, WBLBs, and RBLs) are shared among cells in one column. In this process WWL and RWL are driven independently.

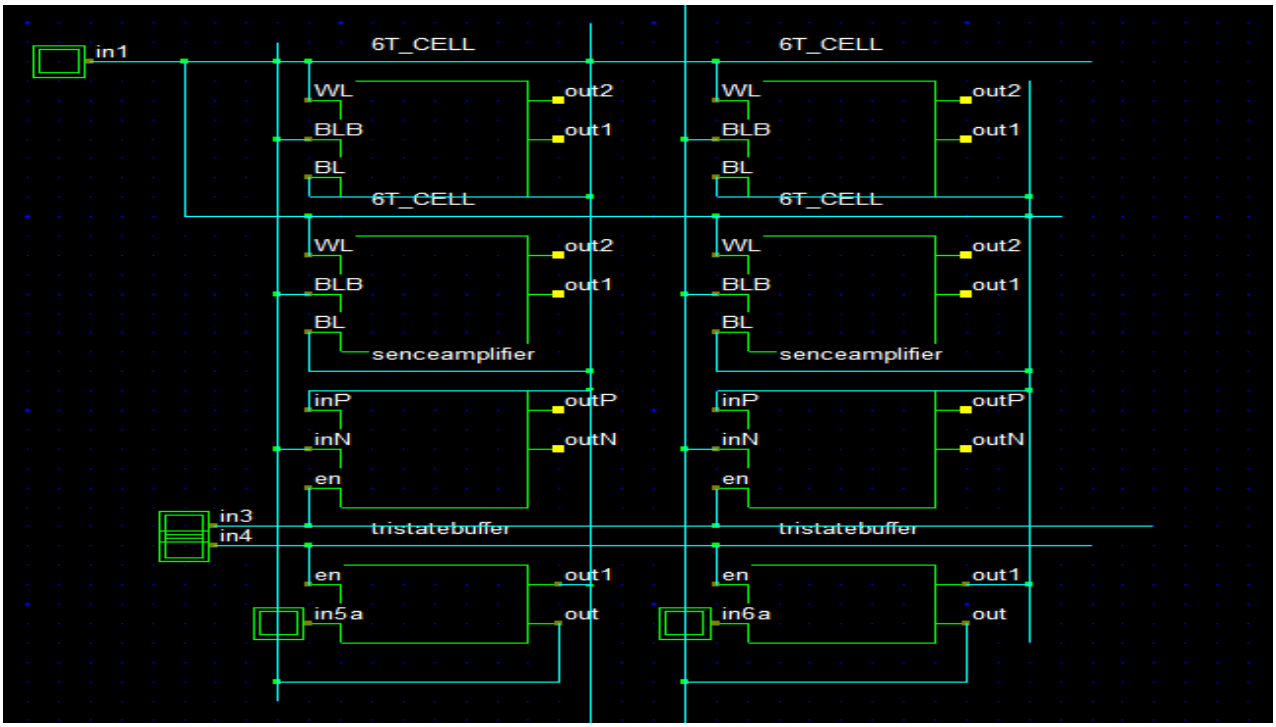

Fig 1.4 2x2 6T SRAM Array

2X2 6T LAYOUT DESIGN

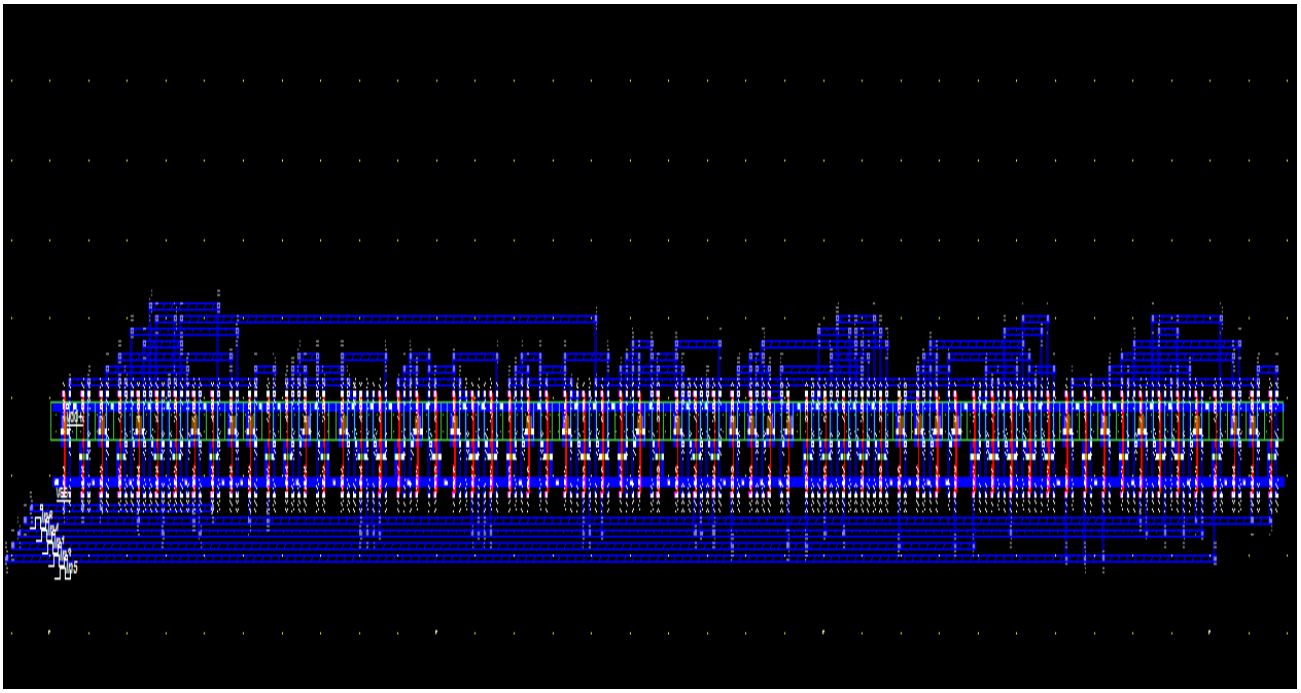

Fig 1.5 2X2 6T LAYOUT DEESIGN

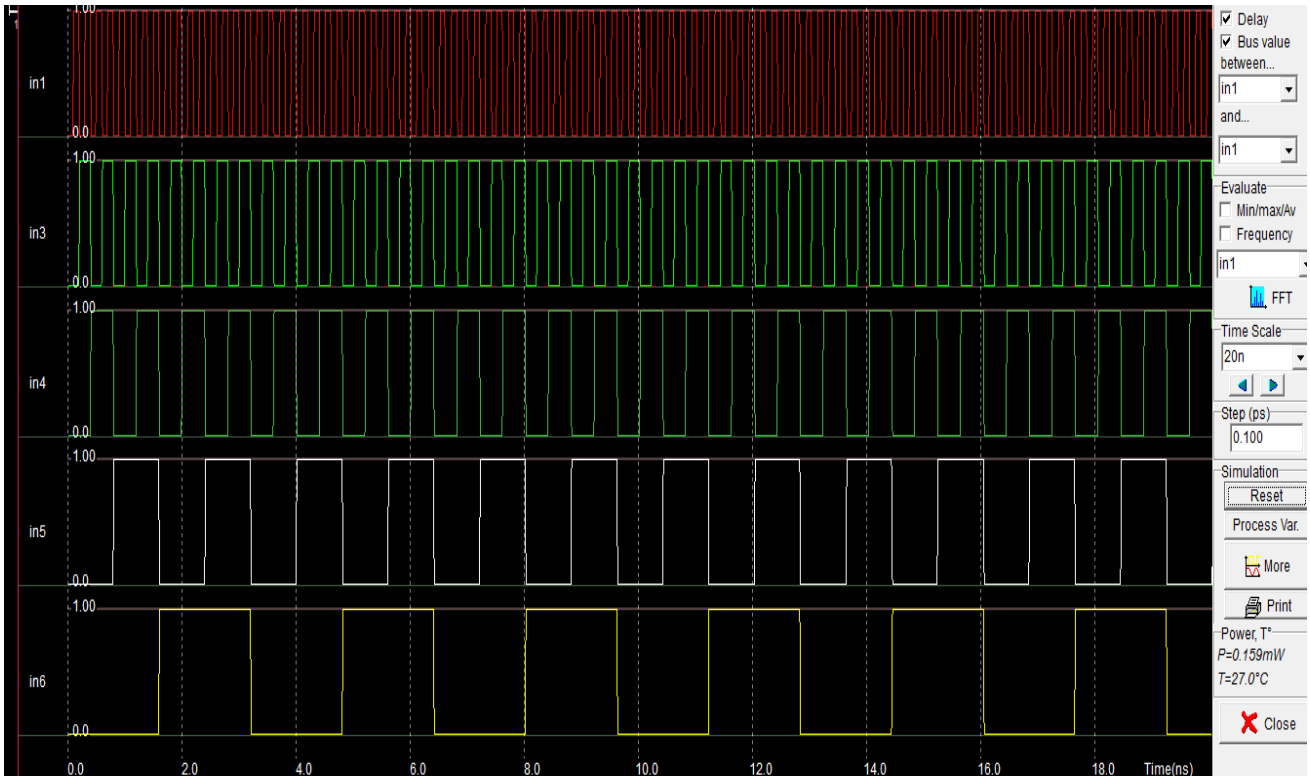

Fig 1.6 2X2 6T LAYOUT DEESIGN

4X4 SRAM ARRAY IMPLEMENTATION

In order to increase the capacity of SRAM cells the array size was increased from 2X2 to 4X4 and the proposed 4X4 array is capable of storing 16 bits data in its memory. Hence the various types (6T, 7T, 8T, 10T and 11T) of SRAM cells are implemented in 4X4 array architecture.

4X4 6T SRAM ARRAY

There are 4 rows and 4 columns arranged to form a 4x4 6T SRAM cell array. Here the WL represents the word line, RD represents the read operation and WR represents the write operation respectively.

4X4 7T ARRAY

The 7T SRAM cell is similar to 6T but the symbol of 6T alone is replaced by 7T array symbol while the sense amplifier and the tristate buffer remaining the same.

4X4 10T SRAM ARRAY

Upon the activation of write enable (WR) signal (represented in the block) activates the write buffer output change according to the input

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V. EXPERIMENTAL RESULTS

Power, Capacitance, Voltage Analysis, Temperature Analysis

Technology	SRAM	Power Consumption	Capacitance In Farad			Voltage in Volts		Temperature in degree celsius		Power Dissipation in Micro Watts
			20	60	100	0.8	1.1	-60	+100	
90	6T	0.0520	0.071	0.068	0.066	0.044	0.082	0.141	0.075	
65		0.0202	0.030	0.030	0.030	0.012	0.027	0.025	0.018	
45		0.0107	0.019	0.031	0.036	0.009	0.018	0.018	0.013	
90	7T	0.172	0.160	0.161	0.160	0.196	0.296	0.537	0.117	
65		0.0638	0.113	0.044	0.039	0.055	0.047	0.113	0.038	
45		0.0476	0.087	0.123	0.149	0.028	0.028	0.033	0.023	
90	8T	0.097	0.148	0.159	0.129	0.050	0.084	0.140	0.100	
65		0.038	0.038	0.036	0.036	0.024	0.046	0.018	0.046	
45		0.027	0.029	0.029	0.029	0.019	0.031	0.0139	0.021	
90	10T	0.0834	0.072	0.067	0.066	0.039	0.063	0.094	0.060	
65		0.0353	0.030	0.030	0.030	0.021	0.034	0.040	0.026	
45		0.0227	0.027	0.033	0.036	0.014	0.022	0.024	0.017	
90	11T	0.0939	0.109	0.149	0.153	0.041	0.083	0.144	0.079	
65		0.0355	0.049	0.064	0.067	0.016	0.029	0.031	0.021	
45		0.0280	0.040	0.054	0.055	0.012	0.021	0.022	0.015	

TABLE I

For 2X2 Analysis

Technology	SRAM	Power Consumption	Capacitance In Farad			Voltage in Volts		Temperature in degree celsius		Power Dissipation in Micro Watts
			20	60	100	0.8	1.1	-60	+100	
90	6T	0.0520	0.071	0.068	0.066	0.044	0.082	0.141	0.075	
65		0.0202	0.030	0.030	0.030	0.012	0.027	0.025	0.018	
45		0.0107	0.019	0.031	0.036	0.009	0.018	0.018	0.013	
90	7T	0.172	0.160	0.161	0.160	0.196	0.296	0.537	0.117	
65		0.0638	0.113	0.044	0.039	0.055	0.047	0.113	0.038	
45		0.0476	0.087	0.123	0.149	0.028	0.028	0.033	0.023	
90	8T	0.097	0.148	0.159	0.129	0.050	0.084	0.140	0.100	
65		0.038	0.038	0.036	0.036	0.024	0.046	0.018	0.046	
45		0.027	0.029	0.029	0.029	0.019	0.031	0.0139	0.021	
90	10T	0.0834	0.072	0.067	0.066	0.039	0.063	0.094	0.060	
65		0.0353	0.030	0.030	0.030	0.021	0.034	0.040	0.026	
45		0.0227	0.027	0.033	0.036	0.014	0.022	0.024	0.017	
90	11T	0.0939	0.109	0.149	0.153	0.041	0.083	0.144	0.079	
65		0.0355	0.049	0.064	0.067	0.016	0.029	0.031	0.021	
45		0.0280	0.040	0.054	0.055	0.012	0.021	0.022	0.015	

TABLE II

These analysis for 2x2 that is 4 bit TSRAM cells for 6T, 7T, 8T, 10T, 11T SRAM cells.

For 4x4 SRAM Cells

Technology	SRAM	Power Consumption	Capacitance in Farad			Voltage in volts		Temperature in degree Celsius		Power Dissipation in Micro Watts
			20	60	100	0.8	1.1	-60	+100	
90	6T(4x4)	1.354	0.626	0.668	0.698	1.351	2.285	0.582	0.625	
65		0.429	0.421	0.421	0.421	1.084	1.691	0.388	0.452	
45		0.297	0.278	0.314	0.339	0.857	1.272	0.242	0.266	
90	7T(4x4)	29.279	28.863	28.863	28.863	96.521	95.595	2.080	18.519	
65		17.764	17.764	17.809	17.820	19.533	20.745	16.350	18.996	
45		13.833	8.863	8.863	8.863	17.457	17.247	9.301	8.233	
90	8T(4x4)	0.820	0.834	0.840	0.843	0.613	0.623	0.634	0.623	
65		0.437	0.455	0.482	0.493	0.291	0.298	0.288	0.298	
45		0.310	0.258	0.267	0.283	0.265	0.269	0.267	0.269	
90	10T(4x4)	4.933	4.976	5.021	5.026	3.412	4.77	3.66	6.473	
65		2.54	2.072	2.12	2.152	1.812	2.138	1.616	2.690	
45		1.920	1.948	1.946	1.948	1.684	2.057	1.274	2.529	
90	11T(4x4)	0.532	1.018	1.083	1.131	0.965	0.965	1.005	0.951	
65		0.301	0.318	0.345	0.356	0.391	0.391	1.619	0.289	
45		0.3	0.404	0.412	0.416	0.301	0.302	0.888	0.294	

TABLE III

The above tabulation shows that 6T, 7T, 8T, 10T, 11T, SRAM cells Power analysis, Capacitance analysis, Voltage analysis, Temperature analysis. In these cells, power of register files are analysed by using DSCH, MICROWIND. These cells designed for 8x8 bits.

8x8 bit Layout design

Fig. 1.7 8x8 bit Layout Design

This design is based on 8x8 bit. It is used to increase the battery life of the products like computer, desktops, and palmtops.

VI. CONCLUSION

In this project Power analysis, Capacitance analysis, Voltage analysis, Temperature analysis, for various SRAM cells are analysed. Those SRAM cells are analysed by using the existing methods but power, Capacitance, Voltage, Temperature of the SRAM cells are reduced. In proposed method those SRAM (2x2) (4 bit), (4x4) (16 bit) are proposed. For 8x8 SRAM cells are also used. In future 128 bits can be proposed by using this SRAM cells. Battery usage can be increased by using this future method.

REFERENCES

[1] Khawar sarfraz and volkan kursun"VLSI Characterization of a low leakage current and high speed 7T SRAM circuit with wide voltage margins" 2013 IEEE computer society symposium.

[2] Kevin Zhang, *Senior Member,* Fatih Hamzaoglu, and Yih Wang, *Member, IEEE"* Low-Power SRAMs in Nanoscale CMOS Technologies" IEEE TRANSACTIONS ON ELECTRON DEVICES", VOL. 55, NO. 1, JANUARY 2008.

[3] Louis.G. Johnson, "Memory", Lecture notes for ECEN 6263, 2005 http://lgjohn.okstate.edu/6263/lectures/memory.pdf.

[4] Nahid Rahman , Gaurav Dhiman and B. P. Singh "Static-Noise-Margin Analysis of Modified 6T SRAM Cell during Read Operation" Int. J. on Recent Trends in Engineering and Technology, Vol. 8, No. 2, Jan 2013

[5] Ik. -J. Chang, J.-J. Kim, S. P. Park, K. Roy, "A 32 kb 10T Sub- Threshold SRAM Array With Bit-Interleaving and Differential Read Scheme in 90 nm CMOS," IEEE Journal of Solid-State Circuits, vol .44, no. 2, pp. 650-658, Feb. 2009.

[6] E. Grossar, M. Stucchi, K. Maex, W. Dehaene, "Read Stability and Write-Ability Analysis of SRAM Cells for Nano meter Technologies, "IEEE Journal of Solid-State Circuits,vol.41,no.11,pp.2577-2588,Nov. 2006.

[7] V. Gupta and M. Anis, "Statistical design of the 6T SRAM bit cell,"IEEE Trans. Circuits Syst. - I, vol. 57, no. 1, pp. 93–104, Mar. 2010.
[8] M. Gangasukanya, P. Asiya Thapaswin , "Design of high performance SRAM cell using 12T MTCMOS Technology" International Journal Of Engineering And Computer Science ISSN:2319-7242 Volume 4 Issue 6 June 2015, Page No. 12480-12485.
[9] J. Rabaey, A. Chandrakasan, B. Nikolic, Digital Integrated Circuits: A Design Perspective.
[10] Gaurav Hemant Patil, Irene Susan Jacob, Dada Bhagwan Sargar, Sneha Revankar, "DESIGN AND IMPLEMENTATION OF SRAM" Proceedings of 22nd IRF International Conference, 22ndMarch 2015, Pune, India, ISBN: 978-93-82702-81-8
[11] N. Weste, D. Harris, A. Banerjee, CMOS VLSI Design: A circuit and system perspective.
[12] J. Kao, S.Narenda, and A.Chandrakasan, "MTCMOS hierarchical sizing based on mutual exclusive discharge patterns,"Proc. DAC, pp.495-500, 1998.

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