Three Phase Multi-Level Inverter Topology with Symmetrical DC-Voltage Sources

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Abstract— In this paper, a novel three phase modular multilevel inverter (MMLI) is proposed. The proposed inverter consists of primary cell and repetitive modular cells which are connected in series arrangement with the primary cell. Therefore, the proposed topology is able to get more output voltages levels number by adding extra modular cells. Both the sinusoidal pulse width modulation (SPWM) and staircases modulation are effectively executed. The proposed inverter is distinguished by several advantages such as: reduction in the number of semiconductor power switches , reduced Dc-voltage sources count, high utilization factor of the used Dc-voltage sources, and the control execution simplicity. Accordingly, the installation cost and size are reduced. It is simulated using MATLAB software package-tool. In addition, a prototype is developed and examined, to verify both control techniques and performance of the topology. Moreover, experimental results are provided to authenticate the simulation results and it show high similarity with it.

Keywords—multilevel inverter; reduced components count; sinusoidal pulse width modulation; low frequency operation.

I. INTRODUCTION

Multilevel inverters [1-2] have been intensively accepted for medium and high-voltage, high-power industrial & research applications [3] and is attracting wide industrial interest. In the recent past, the necessity of required power quality in industry has encouraged the consistent research and development of voltage source multilevel inverters because of higher efficiency with high switching frequency and improved control methods [1,4,5]. They are attractive in terms of reduction in dv/dt stresses, lesser electromagnetic interference and better output waveform with multiple voltage levels close to the sinusoidal waveform and ultimately reduction in THD. Multilevel inverters synthesize better output voltage and current waveforms with reduced harmonics [6] by generating multiple voltage and current levels in output waveform thus, providing unique solution for the desired applications. Multilevel inverter technology is extensively used in various industrial applications such as, hybrid active harmonic filters, reactive power compensation, renewable energy sector, traction, electric vehicles, speed control of single phase as well as three phase induction motors and many more. But they need more number of components such as input DC sources and power electronic devices i.e. Insulated Gate Bipolar Transistors (IGBTs), Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) and the required gate driver circuitry. But their advantages such as low dv/dt, low electromagnetic interference, small size of output filter (as dominant harmonics are significantly reduced), and reduction in THD in output voltages dominates over their limitations. Multilevel inverter topologies are categorized into two main configurations [7]: (1) Single DC-source inverters, for e.g. Neutral-Point-Clamped (NPC) multilevel inverter and Flying Capacitor multilevel inverters and (2) Multi-DC sources inverters, for e.g. Cascaded H-Bridge (CHB) multilevel inverter [8-9]. Further, multi-DC source inverter is classified into Symmetrical (equal DC source) and Asymmetrical (unequal DC source) topologies. Fundamentally, asymmetrical topologies produce more voltage levels as compared to symmetrical topologies keeping same number of DC sources. Recently, asymmetrical topologies are becoming one of the most interested research areas [10-11] in the field of power electronics and applications. The size of these topologies is substantially reduced improving the overall reliability since minimum number of power electronic components and DC sources are used.

II. CONVENTIONAL MULTILEVEL INVERTER TOPOLOGIES

For getting complete understanding and deep knowledge of multilevel inverter technology, it becomes important to discuss the conventional multilevel inverter topologies. A broad classification of multilevel inverter family is shown in Fig.1.

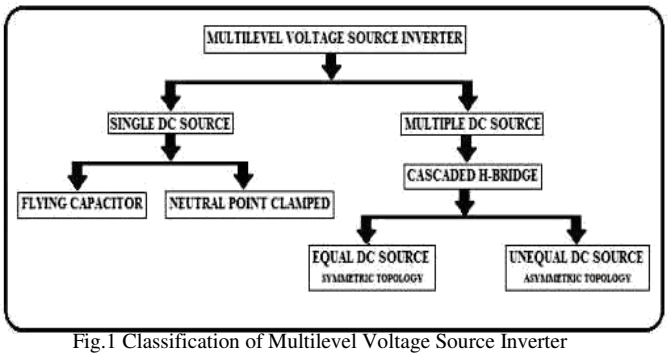

Fig.1 Classification of Multilevel Voltage Source Inverter

A. Diode Clamped Multi-Level Inverter (DCMLI):

The DCMLI [3,12] basically uses the clamping diode to get the desired steps in the output waveform of the inverter. The key concept of DCMLI is the reduction of voltage stress in the power electronic devices with the help of diode. A typical n-level DCMLI requires (n-1) voltage sources, {2(n-1)} switching devices and {(n-1)×(n-2)} diodes [13]. Fig.2 shows the structure of 5-level DCMLI.

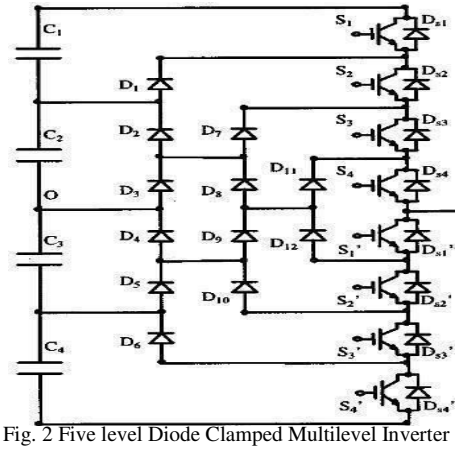

Fig. 2 Five level Diode Clamped Multilevel Inverter

B. Cascaded H-Bridge Multi-Level Inverter (CHBMLI):

It is composed of multiple units of single phase H-bridge power cells; each cell consists of two legs in parallel powered by isolated DC sources. Fig.3 shows the single phase five level CHBMLI.

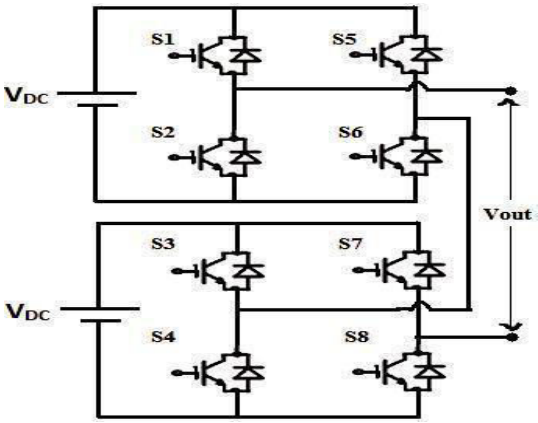

Fig.3 Five level Cascaded H-Bridge Multilevel Inverter

Each leg consists of two series connected power electronics switches. The inverter AC output voltage can be modified by different modulation schemes while its input DC voltage is basically fixed. For achieving the N level with symmetric CHB, it requires {(N-1)/2} number of cells per phase and {2(N-1)} number of switches per phase. Hence for three phase seven level output, it requires nine cells and thirty six switches. The conventional inverters offer few limitations when operating at high frequency because of higher switching losses and the device rating constraints. In view of the above discussions, the techno-economic aspects for the design and development of multilevel inverters are (1) Modular structure

(2) Easy availability (3) Failure management (4) Investment and (5) life cycle cost.

C. Flying Capacitor Multi-Level Inverter (FCMLI):

Five level FCMLI will require {(n-1)×(n-2)/2} clamping capacitors per phase leg in addition to (n-1) main DC capacitors. The voltage stress across each power electronic switch has to be same and equal to {Vdc/(n-1)} for n level multilevel inverter, this is assured by the proper connection of capacitors of FCMLI. But, the major limitation of FCMLI is number of capacitors involved comparative to other multilevel inverter topologies. Fig.4 shows structure of five level FCMLI.

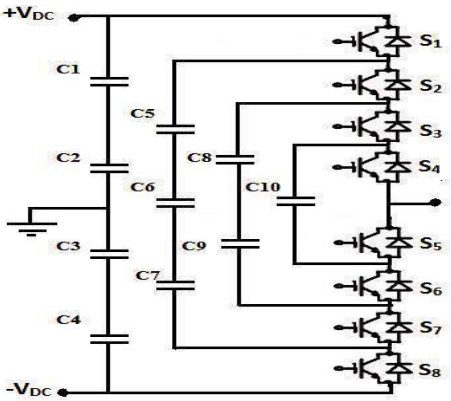

Fig.4 Five level Flying Capacitor Multilevel Inverter

III. SYMMETRIC MULTILEVEL INVERTER TOPOLOGY

This topology presents an asymmetric configuration (input DC sources are of unequal magnitude) for three phase seven level inverter with reduced number of switches. To generate three phase seven level output voltage, the proposed topology requires only twelve switches instead of thirty six switches which are needed in CHBMLI. Fig.5 shows the circuit diagram of the proposed topology simulated in Simu-link. It contains three legs and each leg contains two cells. Each cell contains two complementary switches and one DC source. Magnitude of voltage source in upper cell is 'V' whereas it is '2V' in lower cell. The generated levels of output voltage waveform are: 0Vdc, ±1Vdc, ±2Vdc, ±3Vdc. In simulation 'V' is 150 V and 2V is 300 V, hence generated seven voltage levels are: 0 V, ±150 V, ±300 V, ±450 V. As each phase requires four switches and two voltage sources having different magnitudes, therefore, for three phase output, it requires three voltage sources having magnitude 1Vdc (150 V) and three voltage sources having magnitude 2V (300 V) and twelve switches.

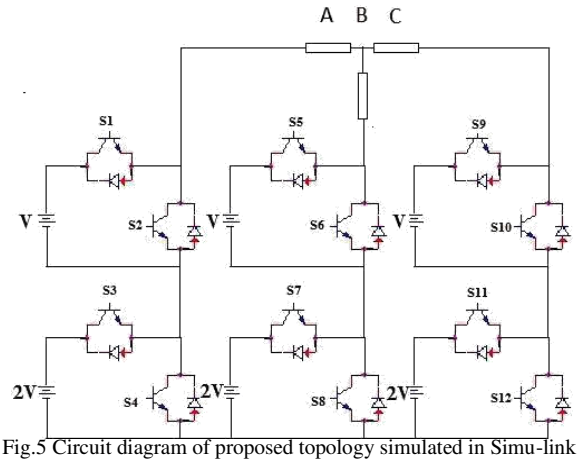

Fig.5 Circuit diagram of proposed topology simulated in Simu-link

For achieving the desired levels, the switches are triggered by a particular well defined pulse pattern. Timing diagram of the desired **pulses for switch S1, S2,…..,S12 is shown in Fig.6.**

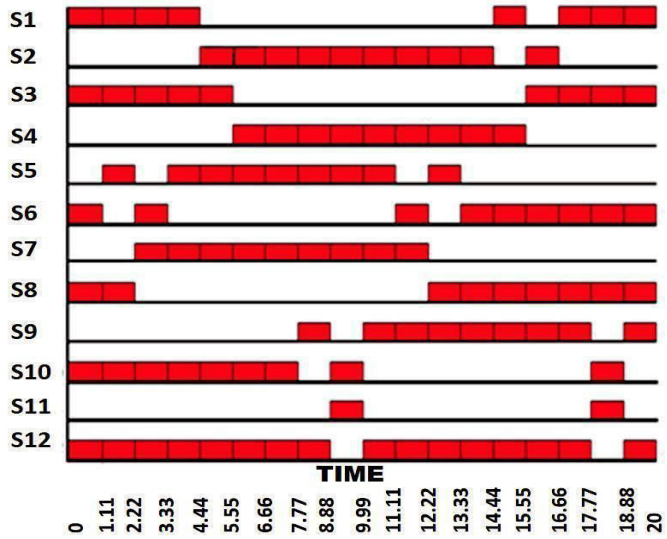

Fig.6 Timing diagram for the asymmetric multilevel inverter topology

It may be noted that according to this pulse pattern, the switches are accordingly switched to obtain the desired seven level output voltage waveform. It can also be clearly observed from the timing diagram that at any instant of time, six switches are ON and six switches are in OFF condition. The switching states for each switch and the corresponding line voltage is shown in Table 1. In three phase voltage waveform when Vab = 0V then Vbc = -3V and Vca = +3V. In order to obtain this state, switches

S2,S4,S6,S8,S9,S11 should be ON and rest switches are OFF. Similarly for achieving other states, particular switches should be ON as shown in switching Table 1.

TABLE 1 SWITCHING STATES FOR THE ASYMMETRIC MULTILEVEL INVERTER TOPOLOGY

SR.	SWITCHING STATES												LINE VOLTAGE		
NO.	S1	S2	S3	S4	S5	S6	S7	S8	S9	S_{10}	S_{11}	S_{12}	V_{AB}	V_{BC}	V_{CA}
1	0	1	0	1	0	1	0	1	1	0	1	0	0	-3V	3V
2	1	0	0	1	0	1	0	1	1	0	1	0	V	-3V	2V
3	0	1	1	0	0	1	0	1	1	0	1	0	2V	-3V	V
4	1	0	1	0	0	1	0	1	1	0	1	0	3V	-3V	0
5	1	0	1	0	0	1	0	1	0	1	1	0	3V	-2V	-V
6	1	0	1	0	0	1	0	1	1	0	0	1	3V	-V	-2V
7	1	0	1	0	0	1	1	0	0	1	0	1	3V	0	-3V
8	1	0	1	0	1	0	1	0	0	1	0	1	2V	V	-3V
9	1	0	1	0	0	1	1	0	0	1	0	1	V	2V	-3V
10	1	0	1	0	1	0	1	0	0	1	0	1	0	3V	-3V
11	0	1	1	0	1	0	1	0	0	1	0	1	-V	3V	-2V
12	1	0	0	1	1	0	1	0	0	1	0	1	-	2V	3V -V
13	0	1		0	1	1	0	1	0	0	1	0	1	-	3V 3V 0
14	0	1		0	1	1	0	1	0	1	0	0	1	-	3V 2V V
15	0	1		0	1	1	0	1	0	0	1	1	0	-3V	V 2V
16	0	1		0	1	0	1	0	1	1	0	1	0	-3V	0 3V
17	0	1		0	1	1	0	0	1	1	0	1	0	-2V	-V 3V
18	0	1		0	1	0	1	0	1	1	0	1	0		-V -2V 3V

IV. CONTROL STRATEGY

In order to obtain desired switching pulse, level shifted multicarrier Pulse Width Modulation (PWM) technique is incorporated. Level shifted means all the carrier waves are displaced by DC offset value of desired magnitude. There are various methods of PWM techniques such as Phase Disposition (PD), Phase Opposition Disposition (POD), and Alternate Phase Opposition Disposition (APOD) through which switching pulses can be obtained [14]. In PD technique, all the carrier waves are in same phase whereas in POD technique, carrier waves above zero reference and 0 below zero reference are phase shifted by 180 . In APOD technique, 0 all the adjacent carrier waves are phase shifted by 180 . In the proposed topology, level shifted PD technique is used [15]. Hence, the PWM technique used is PD in which the entire carrier waves above and below the zero reference are in same phase. The number of carrier waves can be calculated by using {(N-1)/2}, where N is the number of levels of output voltage waveform. Hence, for seven level output voltage waveform, one reference wave and only three carrier waves are required as shown in Fig.7, whereas CHBMLI requires six carrier waves.

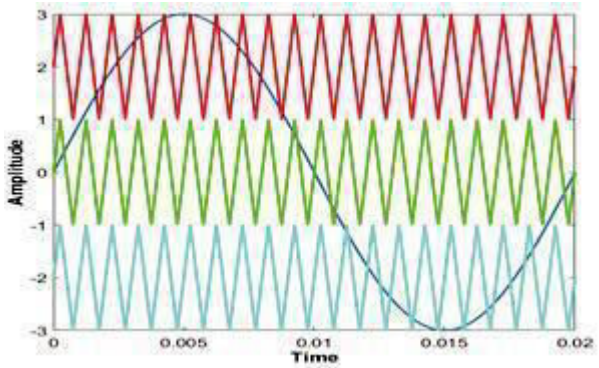

Fig.7 Phase disposition PWM technique

By comparing sine wave with three carrier waves, three different pulse patterns C1, C2, C3 are obtained. Now by using appropriate logic gate circuitry with these three pulses, final gate pulse for switches S1, S2, S3 and S4 are generated for phase A which are G1, G2, G3 and G4 and obtained by using equations (1-4). Thus, the gate signals for switches S1, S2, S3 and S4 respectively are given as shown below [16]:

where, '×' stands for logic AND; '+' stands for logic OR.

In the same way to obtain gate pulses for phase B and C, same carrier waves are compared with the reference sine wave (120^0 phase shifted for phase A and -120^0 for phase C) followed by same logic operation [10]. The modulation index can be obtained by using equation (5) as shown

(5)

where, m = Modulation Index

Am = Peak value of reference sine wave Ac = Peak value of carrier wave

K = No. of levels

V. Simulation Results At Various Modulation Index using Simu-Link

The simulation of the asymmetric multilevel inverter topology has been successfully done for various modulation indices. Fig. 8 -18 shows the THD at various modulation indices with R = 10 ohms, L = 15 mH at 1 kHz carrier frequency.

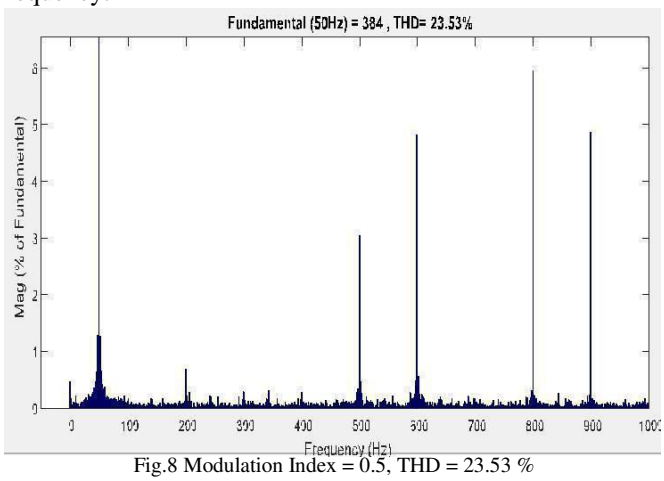

Fig.8 Modulation Index = 0.5, THD = 23.53 %

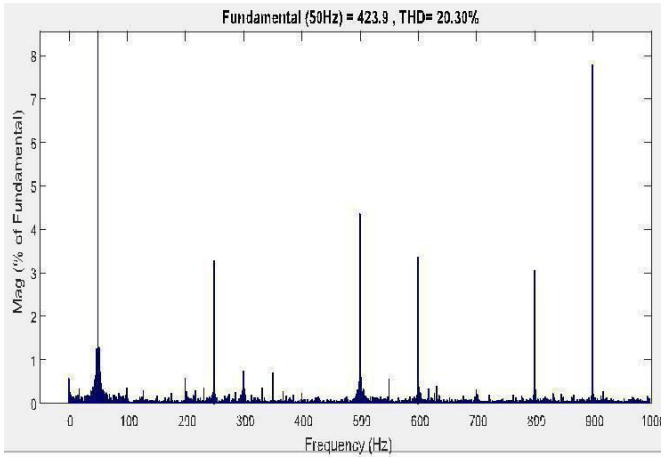

Fig.9 Modulation Index = 0.6, THD = 20.30 %

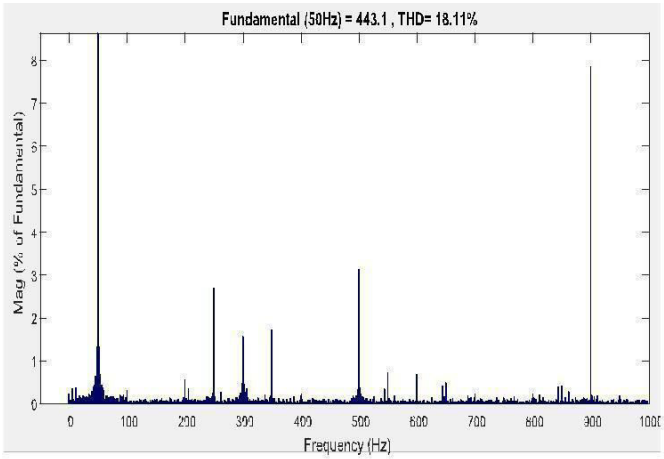

Fig.10 Modulation Index = 0.7, THD = 18.11 %

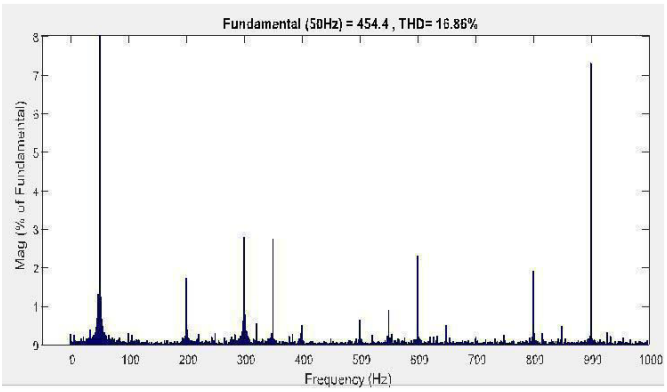

Fig.11 Modulation Index = 0.8, THD = 16.89 %

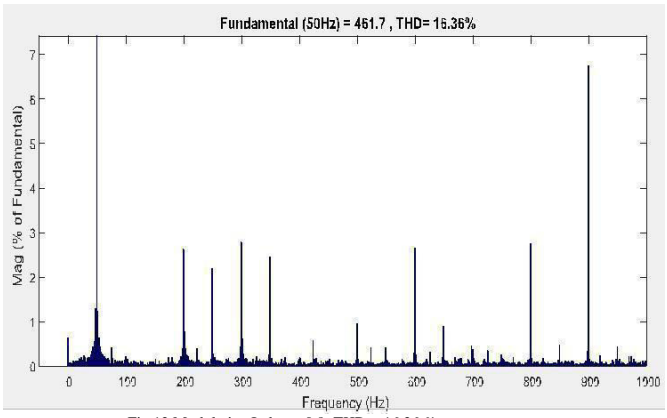

Fig.12 Modulation Index = 0.9, THD = 16.36 %

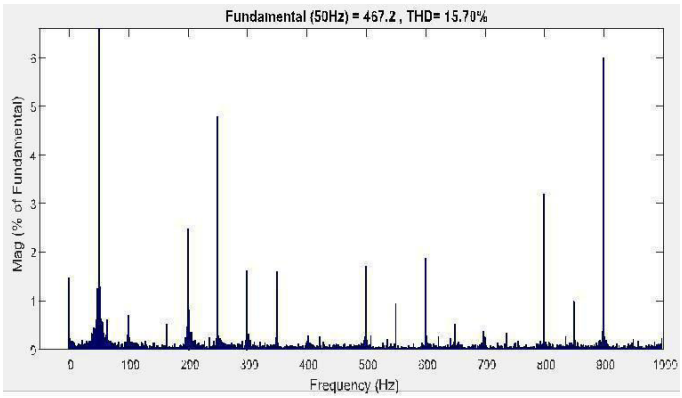

Fig.13 Modulation Index = 1, THD = 15.70 %

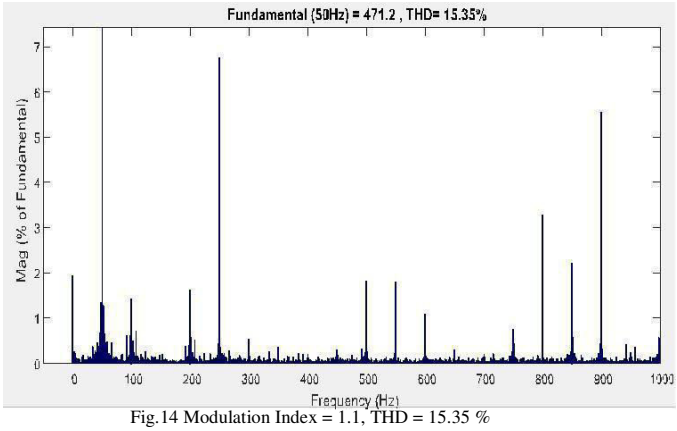

Fig.14 Modulation Index = 1.1, THD = 15.35 %

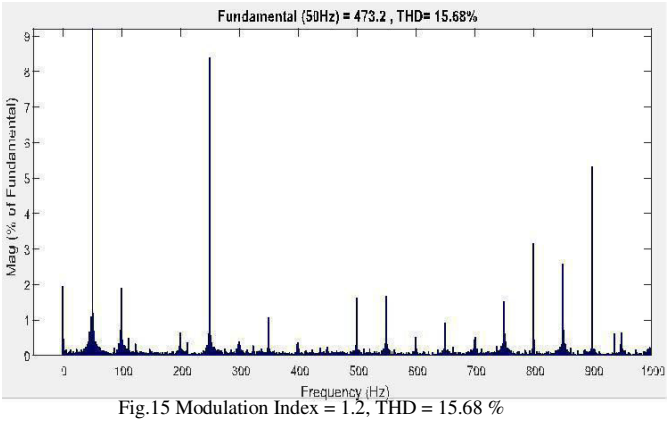

Fig.15 Modulation Index = 1.2, THD = 15.68 %

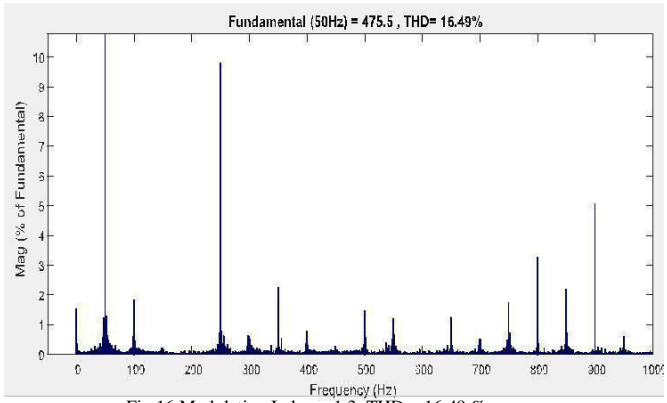

Fig.16 Modulation Index = 1.3, THD = 16.49 %

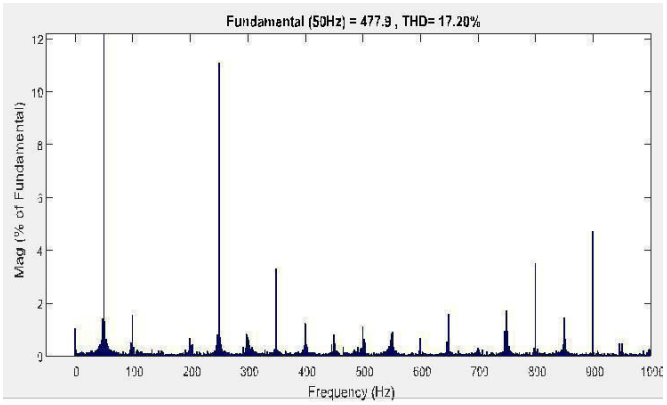

Fig.17 Modulation Index =1.4, THD = 17.20 %

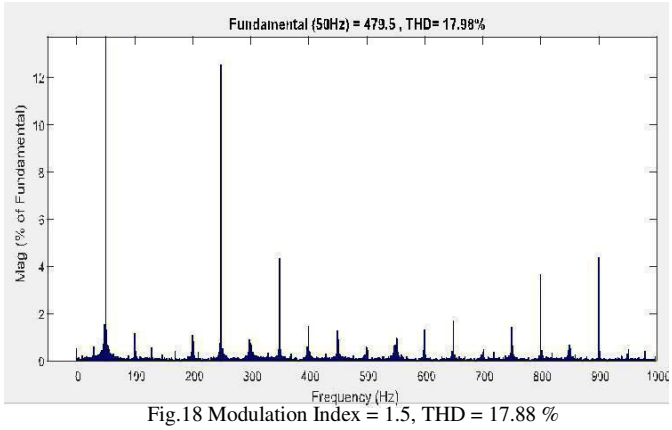

Fig.18 Modulation Index = 1.5, THD = 17.88 %

On the basis of this analysis, the best result obtained at modulation index 1.1 and corresponding THD is 15.35 % by using Simu-Link tool. The topology is simulated at no -load, R-load and RL-load using IGBT as the switching device with the parameters: R=10 ohms, L=15 mH, F c=1 kHz and M i= 1.1. Fig. 19 shows the three phase line to line output voltage waveform for R-load, RL-load and no load. Fig.20 and Fig.21 shows the output current waveform at R-load and RL-load respectively.

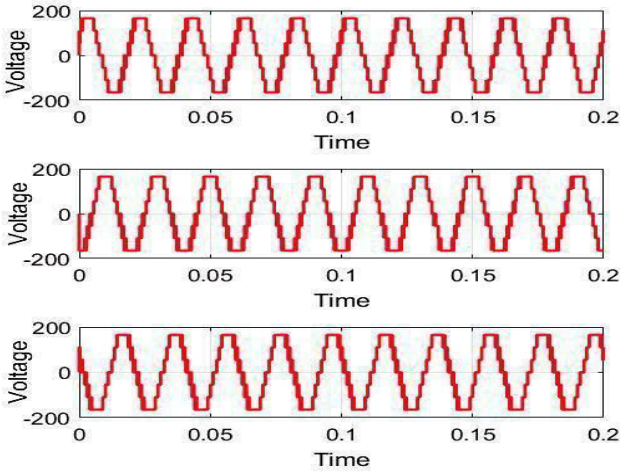

Fig.19 Three phase line to line output voltage waveforms (a) R phase (b) Y phase (c) B phase for No-load, R load and RL load

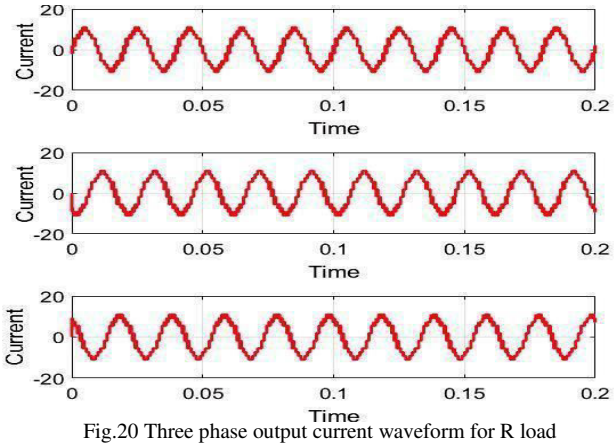

Fig.20 Three phase output current waveform for R load

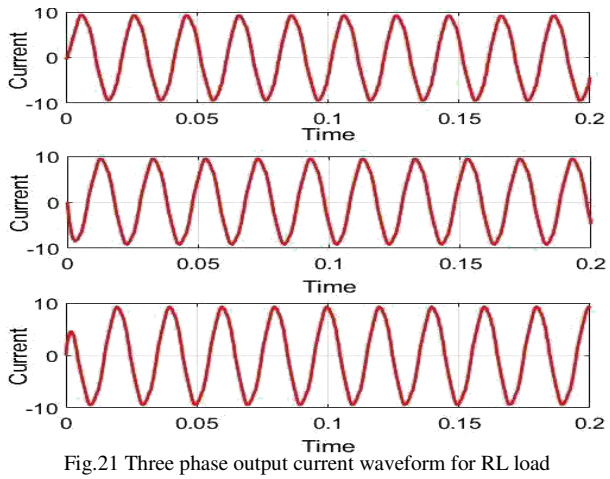

Fig.21 Three phase output current waveform for RL load

VI. COMPARISONS OF VARIOUS MLI TOPOLOGIES

Fig.22 shows the bar graph of THD V modulation index of the proposed MLI topology. From this graph, it can be inferred that the optimal result is obtained at modulation index (M) =1.1 and corresponding minimum THD is 15.35 %.

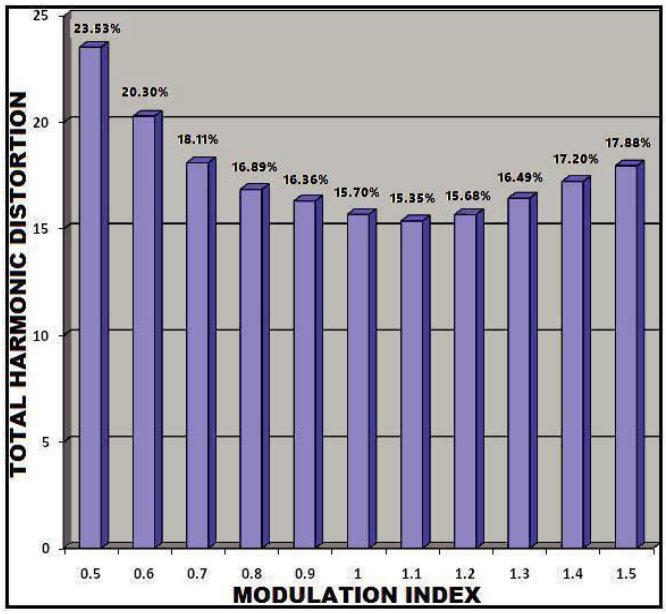

Fig.22 Bar graph of THD V[S] Modulation Index

Table 2 presents the comparison of components used in various three phase seven level MLI topologies which clearly indicates the compactness of the presented MLI topology as the no. of switches and DC sources are much less than the other MLI topologies.

TABLE 2 COMPARISION OF COMPONENTS OF VARIOUS MLI TOPOLOGIES

MLI Topology	No. of Diodes	No. of Capacitors	No. of DC Sources	No. of Switches
Cascaded H Bridge	-	-	9	36
Diode Clamp	90	-	-	36
Flying Capacitor	-	-	63	36
Presented Topology	-	-	6	12

VII. CONCLUSIONS

A three-phase Cascaded Multilevel Inverter with asymmetric topology has been successfully simulated using Simu-Link for various modulation indices. The main motivation of carrying out the analysis is successfully achieved by obtaining an optimum value of the modulation index at minimum THD. With less number of switches and input DC sources, the proposed topology results in reduced installation area. Level shifted Phase Disposition PWM technique is successfully employed for different load conditions. Also from the various simulation results it can be seen clearly that, THD is reduced when modulation index (m) increases from 0.5 to 1.1. Further increment in ' m' causes increment in THD. The optimal result is obtained at m =1.1 and the corresponding THD is 15.35 %. At this optimum value of modulation index, the topology is simulated at no load, R load and RL load conditions. Since, only two DC source are required per phase hence this topology can be utilized with renewable energy and other crucial industrial and research applications. Furthermore, different modulation control strategies can also be implemented for opening new challenges in the field of multilevel inverter technology.

REFERENCES

[1] J. S. Lai and F. Z. Peng, "Multilevel converters — A new breed of power converters," IEEE Trans. Ind. Appl., vol. 32, no. 3, pp. 509–517, May/June 1996.

[2] C. Hochgraf, R. Lasseter, D. Divan and T. A. Lipo, "Comparison of multilevel inverters for static VAR compensation," in Proc. IEEE Ind. Appl. Soc. Annu. Meeting, pp. 921–928, 1994.

[3] T. Ishida, K. Matsuse, T. Miyamoto, K. Sasagawa and L. Huang, "Fundamental characteristics of five-level double converters with adjustable DC voltages for induction motor drives," IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 775–782, Aug. 2002.

[4] Rodriguez J., Jih-Sheng L. and Fang Zheng P., 'Multilevel inverters: a survey of topologies, controls, and applications', IEEE Trans. Ind. Electron., 49, pp. 724–738, 2002.

[5] Colak I., Kabalci E. and Bayindir R., 'Review of multilevel voltage source inverter topologies and control schemes', Energy Convers Manage, 52, (2), pp. 1114–1128, 2011.

[6] C. Rech and J. R. Pinheiro, "Impact of hybrid multilevel modulation strategies on input and output harmonic performance," IEEE Trans. Power Electron., vol. 22, no. 3, pp. 967–977, May 2007.

[7] G. J. Su, "Multilevel DC-link inverter," IEEE Trans. Ind. Appl., vol. 41, no. 3, pp. 848–854, May–June 2005.

[8] M. Malinowski, K. Gopakumar, J. Rodriguez and M. A. Pérez, "A survey on cascaded multilevel inverters," IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2197–2206, July 2010.

[9] D. Baimel and S. Tapuchi, "A new topology of cascaded multilevel inverter," in Proc. Int. Symp., pp. 137–140, Sep. 2013.

[10] H. Belkamel , S. Mekhilef, A. Masaoud and M. A. Naeim, "Novel three-phase asymmetrical cascaded multilevel voltage source inverter," IET Power Electron., vol. 6, no. 8, pp. 1696–1706, Sep. 2013.

[11] M. Veenstra and A. Rufer, "Control of a hybrid asymmetric multilevel inverter for competitive medium-voltage industrial drives," IEEE Trans. Ind. Appl., vol. 41, no. 2, pp. 655–664, March/April 2005.

[12] Y. S. Lai and F. S. Shyu, "Topology for hybrid multilevel inverter," IEE Proc. Elec. Power Appl., vol. 149, no. 6, pp. 449–458, Nov. 2002.

[13] Nabae, I. Takahashi and H. Akagi, "A new neutral-point-clamped PWM inverter," IEEE Trans. Ind. Appl., vol. IA-17, no. 5, pp. 518–523, Sep. 1981.

[14] P. R. Kumar, R. S. Karthik, K. Gopakumar, J. I. Leon and L. G. Franquelo, **"**Seventeen-level inverter formed by cascading flying capacitor and floating capacitor H-bridges,**"** IEEE Trans. Power Electron., vol. 30, no. 7, pp. 3471–3478, July 2015.

[15] V. Goel, J. Kumar and J. Gambhir, **"**Different multilevel inverter topologies with reduced number of devices**"**, 2nd IEEE International conf. on recent advances in engineering & computational sciences**"**, 2015.

[16] N. Seth, R.D Kulkarni and V.P Joshi, **"**Three Phase Asymmetric Multilevel Inverter with Reduced number of Switches for Improved Harmonic Performance**"**, International Journal of Engineering Research & Technology, vol. 5, no. 01, January 2016.