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Area and Power Efficient Pass Transistor Based (PTL) Full Adder Design

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Abstract – **The full adder performs addition of numbers and is an essential component in the design of digital signal processors, microprocessors and controllers. This paper describes the design of Pass Transistor logic based full adder circuit design. This circuit is designed based on XOR and XNOR. The proposed circuit is designed and simulated in Microwind version 3.1 tool of 32 nano meter technologies. From simulation results it is observed that in proposed design power dissipation is reduced from microwatts to nano watts and more than 50 % of area is reduced.**

Keywords: Full adder, PTL, GDI, Transistor, CMOS, PMOS, NMOS

I. INTRODUCTION

Addition is a fundamental operation for any digital system, like, digital signal processors and control system. A quick and accurate operation of a digital system is greatly influenced by the performance of the resident adders because of their extensive use in other basic digital operations such as subtraction, multiplication and division. The design criterion of a full adder cell is usually a multi fold. Transistor count is a primary concern which largely affects the design complexity of many functional units like gate, multiplexer and ALU. The limited power supply capability of battery technology as made power consumption an important figure in small size devices. There is no ideal full adder cell that can be used in all types of applications [1].More number of PMOSs also reduces the speed of the design. Variety of logic styles have been used to design full adders, for example CMOS full adder [2].The main drawback of static CMOS circuits is the existence of PMOS block, because of its low mobility compared to the NMOS devices. PMOS devices need to be seized up to attain the desired performance. Further in CMOS adders more number of transistors are required to realize XOR- XNOR gates resulting in complex design and increasing the chip area. Energy efficient adders [3] [4] [5] [6] though have low Power delay product (PDP) but still consumes a significant area. Another conventional adder is the complimentary pass transistor logic.

II. LITERATURE SURVEY

In [7] adder cell is designed using 28 transistors using standard CMOS technology. Due to more number of transistors power consumption is more. Large PMOS transistor in pull up

network result in high input capacitances which cause more delay and dynamic power. The major advantage of this adder is high noise margin and reliable operation. In [8] adder is constructed using 6 multiplexers and 12 transistors. Each multiplexer is implemented by pass transistor logic with 2 transistors. There is no V_{DD} or ground connection in this circuit and there are some paths containing 3 serried transistors. This increase delay of producing SUM signal. The size of each transistor in mentioned path should be 3 times larger to balance the output and optimize the circuit for Power delay Product (PDP), then the area of the circuit increases.in [9] 10 transistor (10 T) adder cell, the implementation of XOR and XNOR of A and B is done using pass transistor logic and an inverter is to compliment the input signal A. This implementation results in faster XOR and XNOR outputs and also ensures that there is a balance of delay at the output of these gates. This leads to spurious SUM and carry signals. The energy recovering logic reuses charge and hence consume less power than non-energy recovering logic. In this design adder has no direct path to the ground, this reduce power consumption. The charge stored at load capacitance is resupplied to the control gates. Thus adder becomes an energy efficient design. But major disadvantage of this circuit is that it cannot be cascaded at low power supply due to multiple threshold problems. In [10] the static energy recovery XNOR gate is cascaded with the new G-XNOR gate to generate the SUM while the C_{oot} function is implemented by simply multiplexing B and C_{an}. This adder consumes less power in high frequencies and have higher speed adder. However with same power consumption it performs faster.

III. PROPOSED DESIGN

The proposed pass transistor logic (PTL) is to use purely NMOS pass transistor network for logic operation. In this design, transistor acts as switch to pass logic levels from input to output and thus design requires less transistor count because one pass transistor network (either NMOS or PMOS) is enough to perform the necessary logic operation. Speed is increased because of less number of transistors. PTL based full adder design has some advantages over static CMOS that it has the capability to implement a logic function with a smaller number of transistors. Smaller area and less power consumed. The performance of the proposed adder is compared with GDI 10T full adder and GDI 11T full adder.

Proposed design XOR-XNOR module has been made by 3 NMOS and 2 PMOS transistors (figure 1) which provide an area efficient circuit design as compared to previous discussed design models. MOS logic states on four different input combination has been shown in table 1 for both XOR and XNOR output. Comparative analysis of proposed XOR-XNOR module in terms of area with other existing XOR-XNOR module has been shown in Table1.

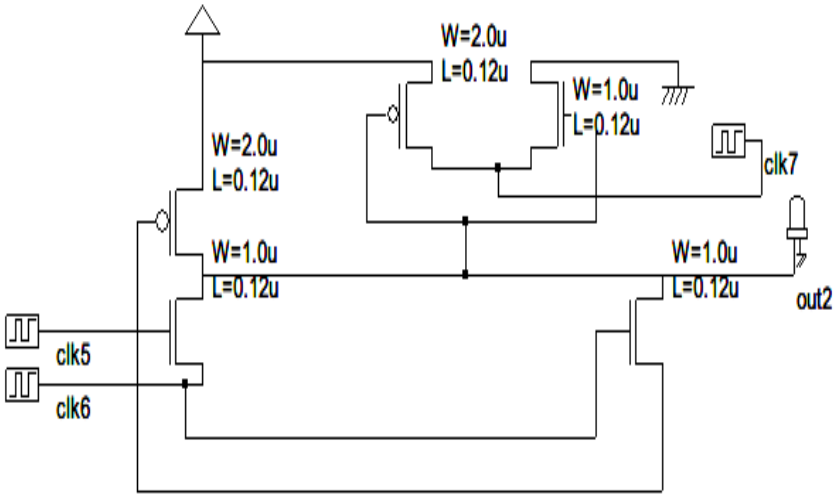


Figure 1: proposed PTL based XOR-XNOR Module

A	B	N1	N2	N3	P1	P2	A xor B	A xnor B
0	0	OFF	OFF	ON	ON	OFF	0	1
0	1	OFF	ON	OFF	ON	ON	1	0
1	0	ON	OFF	OFF	OFF	OFF	1	0
1	1	ON	ON	ON	OFF	OFF	0	1

TABLE: 1 ANALYSIS OF PROPOSED XOR-XNOR MODULE

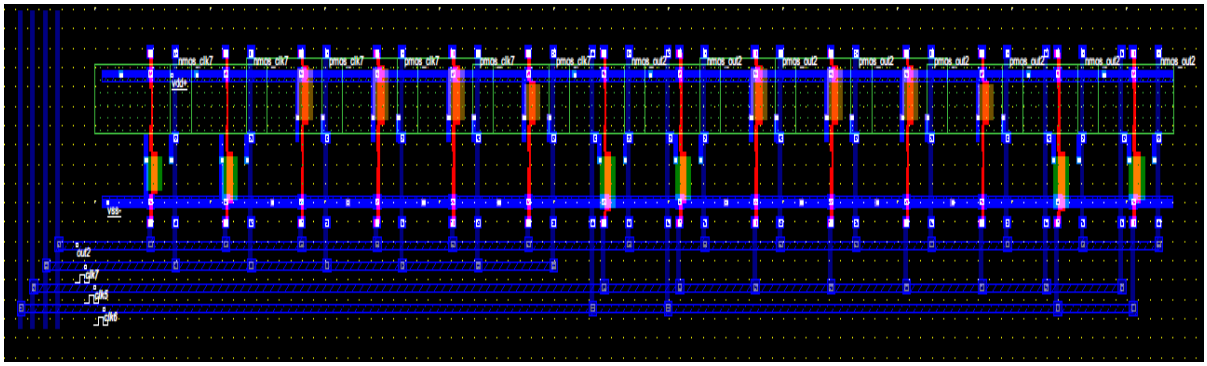


Figure 2: Layout of proposed PTL based XOR-XNOR Module in Microwind version3.1

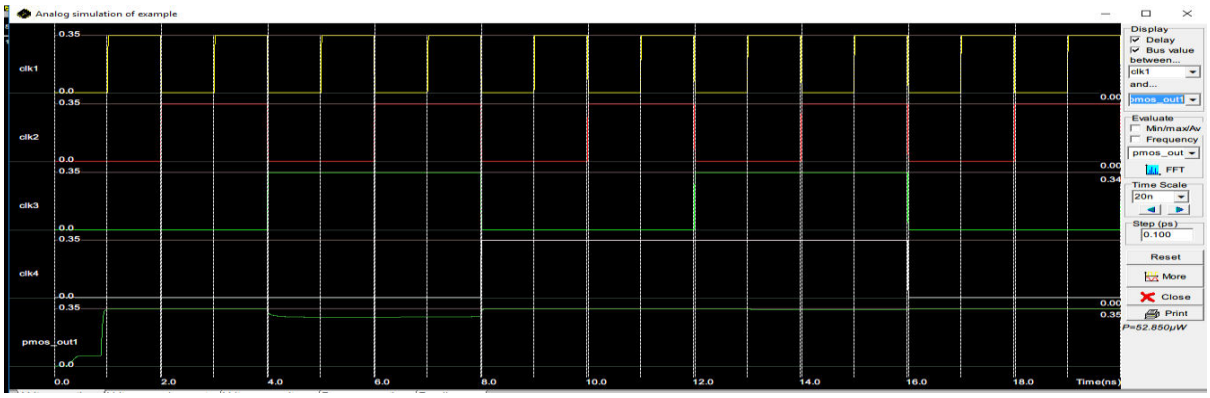


Figure 3: Layout of proposed PTL based XOR-XNOR Module Voltage Vs time diagram

Verification and simulation of the functionality of proposed XOR-XNOR module is first done by using DSCH 3.5 designing tool. Channel width should be accurate for efficient working of the design. Channel width can be changed in DSCH schematic editor. The timing simulated for 5T XOR –XNOR module will show the accurate functioning of the proposed design. The 5T XOR-XNOR module has been compared with the previous discussed XOR-XNOR deigns in terms of area in Microwind designing tool. Microwind deals with both front end and back end designing. In front end it has DSCH in which both transistor level and gate level designing can be done. DSCH generate a Verilog file which can be compiled by the Microwind back end designing tool to get power and area consumption. The 5T XOR-XNOR module is compared with the discussed XOR-XNOR designs in terms of area on 32nm technology.

Outputs of module 1 act as inputs for the module 2 and module 3. The logical Boolean expression for module 2 and 3 can be expressed as:

$$SUM = C\ (A\ xnor\ B) + C\ bar\ (A\ xor\ B)\ CARRY = C\ (A\ xor\ B) + A\ (A\ xnor\ B)$$

The major difference between CMOS and Gate Diffusion Input (GDI) is that the input of the PMOS in a GDI cell is not connected to supply voltage (V_{DD}) and the input of NMOS i snot connected to ground. This causes two extra input pins for making GDI design more comfortable than CMOS design .This technique helps to reduce power consumption, delay and area of digital circuits while maintaining low complexity of logic design GDI technique is an efficient technique for designing area and power efficient digital circuits as compared to PTL, TG, CPL and DPL designing approaches. Schematic of proposed full adder has been designed and simulated in DSCH 3.5 logic editor and simulator.GDI 10T full adder circuit is shown in the figure 4.figure describes that how XoR gate is implemented in GDI technique. It is the main building block of full adder circuit. Optimizing XoR gate overall performance of GDI 10 T full adder can be improved.

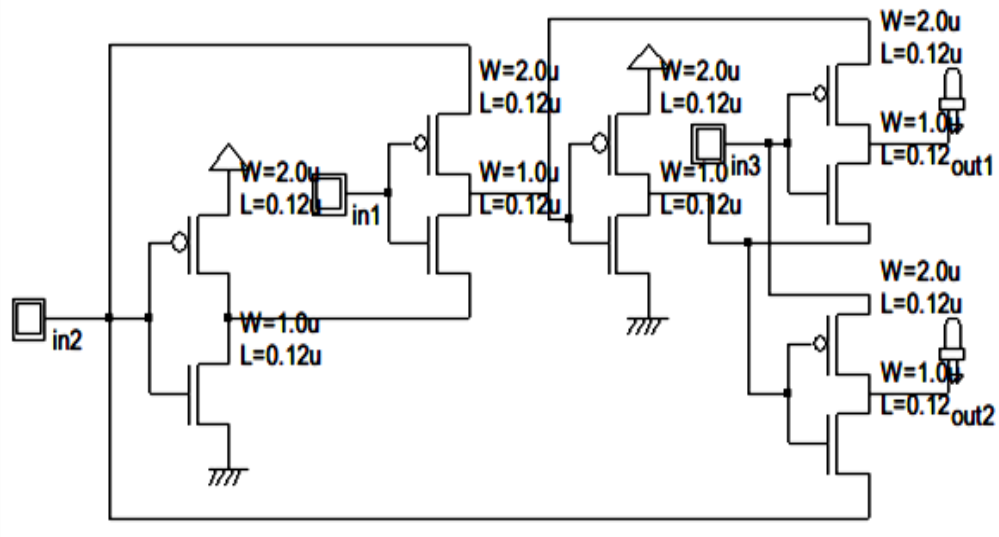


Figure 4: Block diagram of 1 bit full adder (10T) using GDI technique

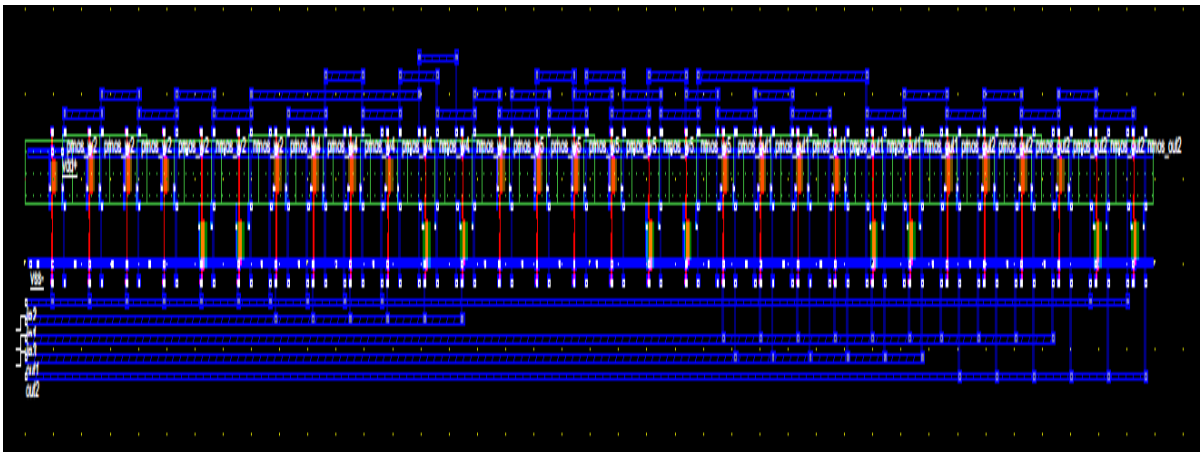


Figure 5: Layout of GDI 10 T full adder Module in Microwind version3.1Figure

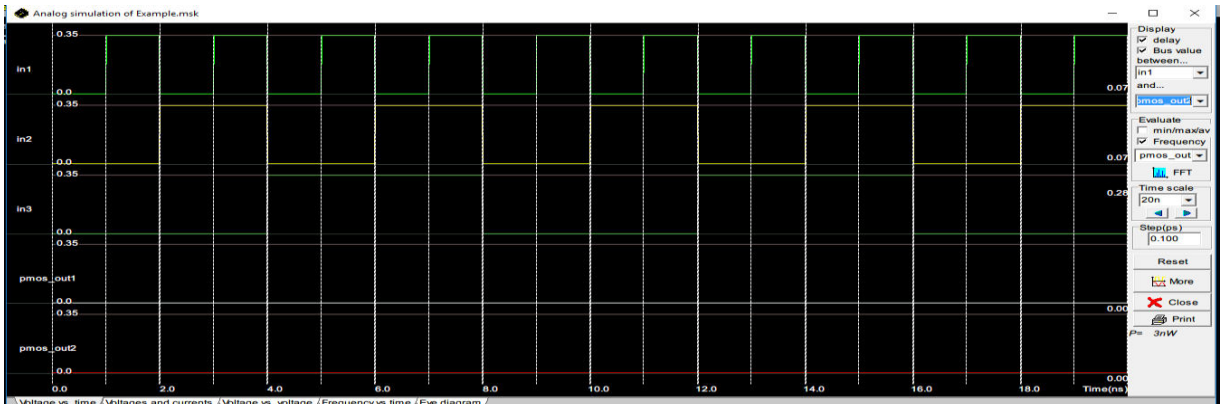


Figure 6: Layout of GDI 10 T full adder Module Voltage Vs time diagram

The GDI 11T full adder is shown in the figure 7.The sleep transistor is connected to the ground and is responsible for the average power consumption reduction of the circuit. when the circuit is in active mode sleep transistor will be in off state and when circuit is in standby mode the sleep transistor will be in ON state. GDI 11T full adder reduces power consumption and the delay of the circuit compared to GDI 10T based full adder circuit

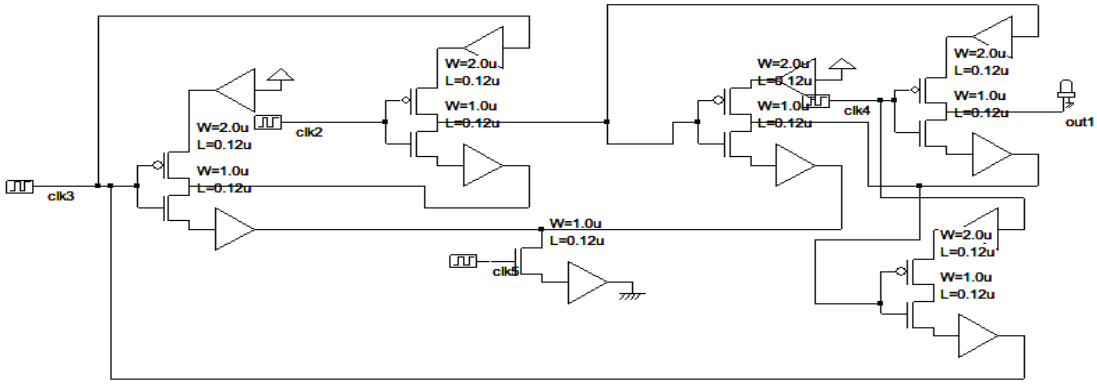


Figure 7: GDI 11 T full adder schematic

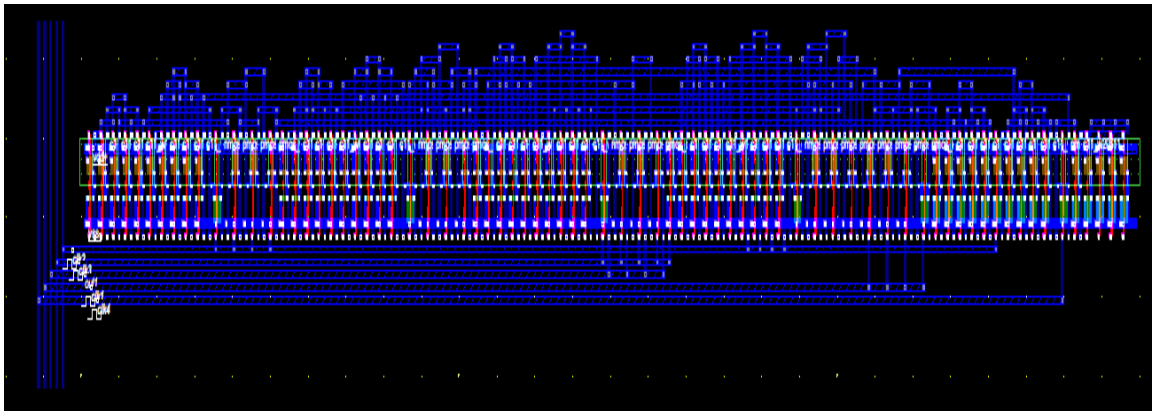


Figure 8: Layout of GDI 11 T full adder Module in Microwind version3.1Figure

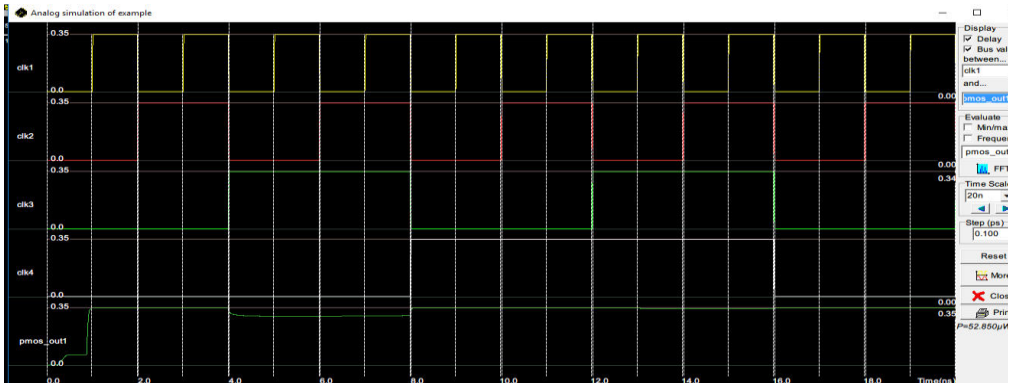


Figure 9: Layout of r5yi GDI 10 T full adder Module Voltage Vs time diagram

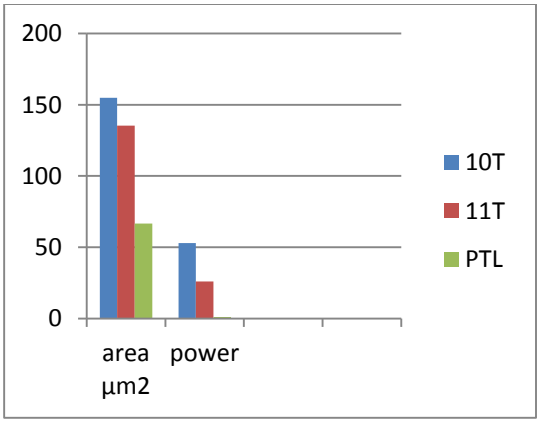
IV. Simulation Results

	area μm^2	Power consumed	NMOS devices	PMOS devices	Electrical nodes	Memory usage
10T	155	52.850 µW	10	20	41	18.3 %
11T	135.3	26 µW	27	27	36	18.3 %
PTL based	66.7	1nW	6	8	21	7.9 %

TABLE 2: PERFORMANCE COMPARISON OF GDI 10T, GDI 11T AND PTL BASED FULL ADDER

The performance of the design is evaluated based on their area, power dissipation and speed. All the simulations are conducted using Microwind version 3.1.All the results are measured using MOS empirical level 3 at 0.35 V and the operating temperature is 27 ^{0}C.The adder ensures an optimum performance for frequency range between 2 MHz to 400 MHz All the results were simulated and analyzed in the range of 50 MHz to 200 MHz. Table 2 compares the performance of GDI 10 T full adder, GDI 11 T Full adder and PTL based full adder. From table 2 it is obvious that PTL based full adder is out performing 10 T and 11 T GDI based full adders in terms of area, power dissipation and speed. As number of PMOS transistors are reduced in the circuit the speed of the PTL based full adder circuit is greatly increased.

- PTL based full adder has 58.6% of reduction in area over GDI 10T and GDI 11T full adders
- In PTL based full adder circuit power dissipation is reduced from microwatts to Nano watts
- In PTL based full adder PMOS transistors are reduced to 8 .This is 60 % and 70 % reduction over GDI 10 T and GDI 11T full adders



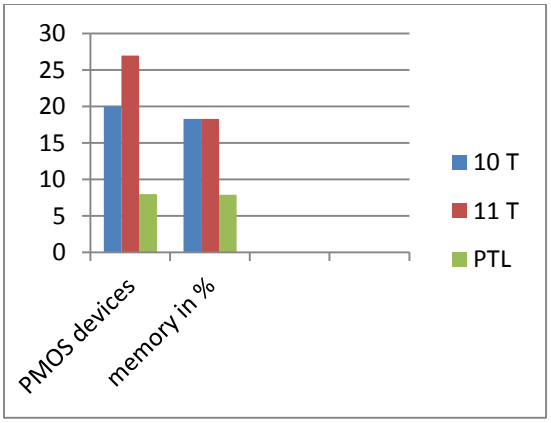


Figure 10: area and power comparison Figure 11: Comparison of PMOS devices and memory

V. CONCLUSION

In this paper PTL based full adder circuit is designed and its performance is compared with GDI 10T, GDI 11T based full adders. PTL based full adder circuit is showing superior performance over 10T and 11T full adders in related to area, power, memory and number of PMOS devices .i.e. speed.

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