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Designing and Analysis of 8 bit SRAM Cell with 32nm CMOS Technology

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Abstract- In this paper an SRAM cell is designed with reduced transmitter count at 32 nm technology. The proposed design is showing better performance interims of power, area and memory.100% of improvement is achieved in power dissipation when compared to Schmitt trigger based SRAM. The proposed SRAM is designed and simulated in DSCH and Microwind 3.1.

Keywords: DSCH, Microwind, Schmitt trigger, SRAM, power, area.

I. INTRODUCTION

Static RAMs are used extensively in modern processors as on chip memories due to their large storage density and small access latency. Low power on-chip memories have become the topic of substantial research as they can account for almost half of total CPU dissipation, even for extremely power-efficient designs. However, static power dissipation is becoming a significant fraction of the total power. Static power is the power dissipated in a design in the absence of any switching activity and is defined as the product of supply voltage and leakage current. The absolute and the relative contribution of leakage power to the total system power is expected to further increase in future technologies because of the exponential increase in leakage currents with technology scaling. The International Technology Roadmap for Semiconductors (ITRS) predicts that leakage power would contribute to 50% of the total power in the next generation processors. Here we present some VLSI techniques to reduce leakage power. Each technique provides an efficient way to reduce leakage power, but disadvantages of each technique limit the application of each technique. In this paper SRAM cell was designed with each technique and analyze the power consumption in each technique.

SRAM to be one of the most fundamental and vitally important memory technologies today. Because they are fast, robust, and easily manufactured in standard logic processes, they are nearly universally found on the same die with microcontrollers and microprocessors. Due to their higher speed SRAM based Cache memories and System on-chips are commonly used. Due to device scaling there are several design challenges for nanometer SRAM design. Low power SRAM design is crucial since it takes a large fraction of total power and die area in high performance processors. A SRAM cell must meet the requirements for the operation in submicron/nano ranges. The scaling of CMOS technology has significant impacts on SRAM cell random fluctuation of electrical characteristics and substantial leakage current. The schematic of SRAM cell is shown in the Fig.1. It has 2 pull up PMOS and 2 NMOS pull

down transistors as two cross coupled inverters and two 2 NMOS access transistors to access the SRAM cell during Read and Write operations. Both the bit lines (BL and BLB) are used to transfer the data during the read and write operations in a differential manner. To have better noise margin, the data signal and its inverse is provided to BL and BLb respectively. The data is stored as two stable states, at storing points VR and VL, and denoted as 0 and 1.

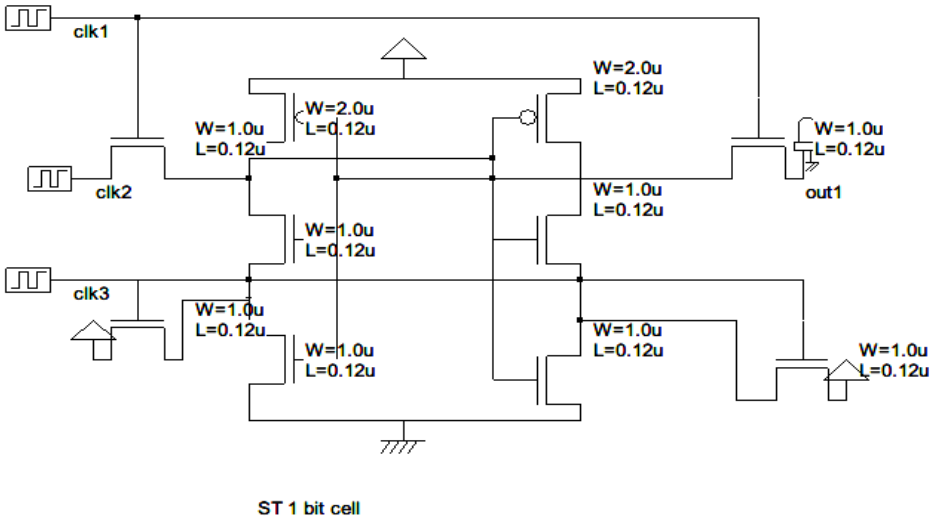

Fig.1: 6T SRAM Cell

II. NEED OF SCHMITT TRIGGER BASED SRAM DESIGNS

In order to resolve the conflicting read versus write design requirements in the conventional 6T bitcell, we apply the Schmitt Trigger (ST) principle for the cross-coupled inverter pair. A Schmitt trigger is used to modulate the switching threshold of an inverter depending on the direction of the input transition. In the proposed ST SRAM bitcells, the feedback mechanism is used only in the pull-down path. During input transition, the feedback transistor (NF) tries to preserve the logic "1" at output (Vout) node by raising the source voltage of pull-down nMOS (N1). This results in higher switching threshold of the inverter with very sharp transfer characteristics. Since a read-failure is initiated by an input transition for the inverter storing logic "1," higher switching threshold with sharp transfer characteristics of the Schmitt trigger gives robust read operation. For the input transition, the feedback mechanism is not present. This results in smooth transfer characteristics that are essential for easy write operation. Thus, input-dependent transfer characteristics of the Schmitt trigger improves both read-stability as well as write-ability of the SRAM bitcell. Two novel bitcell designs are proposed. The first ST-based SRAM bitcell has been presented in our earlier work. Another ST based SRAM bitcell which further improves the bitcell stability has been reported in existing works. To maintain the clarity of the discussion, the ST Bitcell in is termed the "ST-1" bitcell while the other ST Bitcell is termed the "ST-2" bitcell shown in the figure 1

A conventional 6TSRAM cell design consists of a cross-coupled inverter pair (M3-M6) that does data storage and two access transistors (M1-M2) to load/retrieve data on bit lines,

BL and BLB. During a write operation, the data is loaded on the bit lines and the word select signal WS is turned high. A successful write operation occurs if the data is correctly latched in the cell. The bit lines are pre-charged to the supply voltage and the word select line is turned high to retrieve data during a read operation. The bit line (BL) connected to the storage node (V1) storing a „0" gets discharged. The storage node (V1) rises above „0" during a read operation due to voltage division between the access transistor (M1) and the driver transistor (M6). A read failure can occur if the voltage drop rises higher than the threshold voltage of the inverter (M3, M5).

A conventional 6T-SRAM cell provides poor read stability since the access transistors provide direct access to the cell storage during a read operation. The proposed design (see Fig. 4) removes the access hazard during a read operation and therefore eliminates the chances of cell content being inadvertently flipped. It consists of a cross-coupled pair (M3-M6) for data storage as in case of a conventional 6T-SRAM cell. However the ground terminal of the inverter pair is connected to a virtual ground (Gnd_vir1) in the proposed design to provide high speed low-power write operation. The word select line „WS" is held high only during a write operation to load new data in the cell by turning on the write access transistors (M1-M2). A read access transistor (M7) connected to a virtual ground (Gnd_vir2) is used to retrieve data on read bit line (BLR) during a read operation. Our design decouples read/write operation using separate read/write access transistors. Therefore it doesn't suffer from constrained read/write requirements as in 6T-SRAM design.

III. PROPOSED 8T-SRAM

As the Schmitt trigger based designs are having high number of transistor to make the read stability that is 10 Transistor which very high when compared to the existing 6T SRAM Design we are going to combine the mentioned read stability at the above part to our proposed work to reduce the count than the Schmitt trigger based designs at the same time we are going to achieve reduced power consumption with reduced transistor count without affecting the read stability. At the same time the 8T-SRAM design supports separate read and write operations as in the Schmitt Trigger based designs. Our idea is to combine these two different technologies & to design a new circuit with much efficiency than the existing two designs

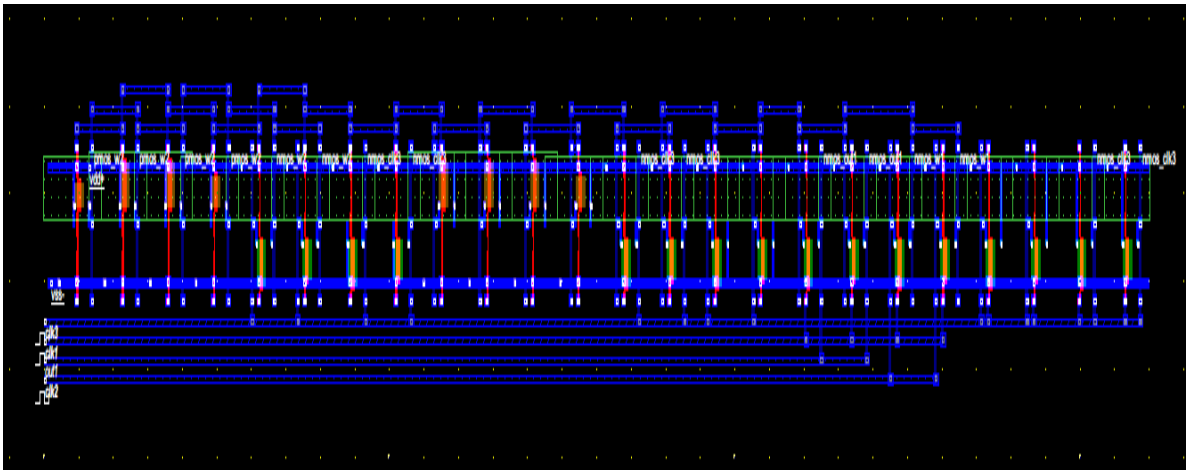

Fig. 2: Layout of ST 1 bit SRAM cell

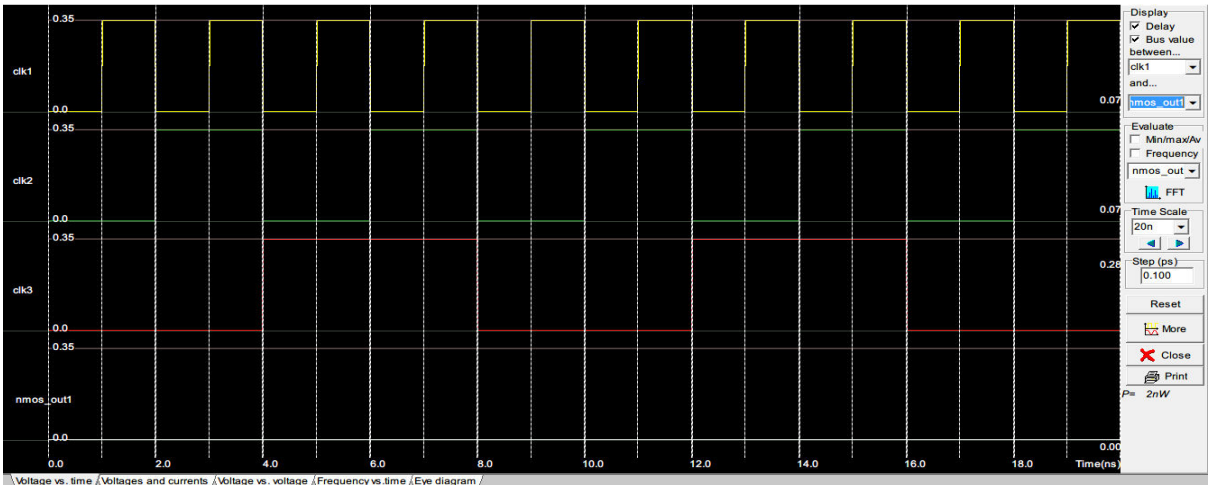

Fig. 3: Time Vs Voltage Graph of 1 bit SRAM cell

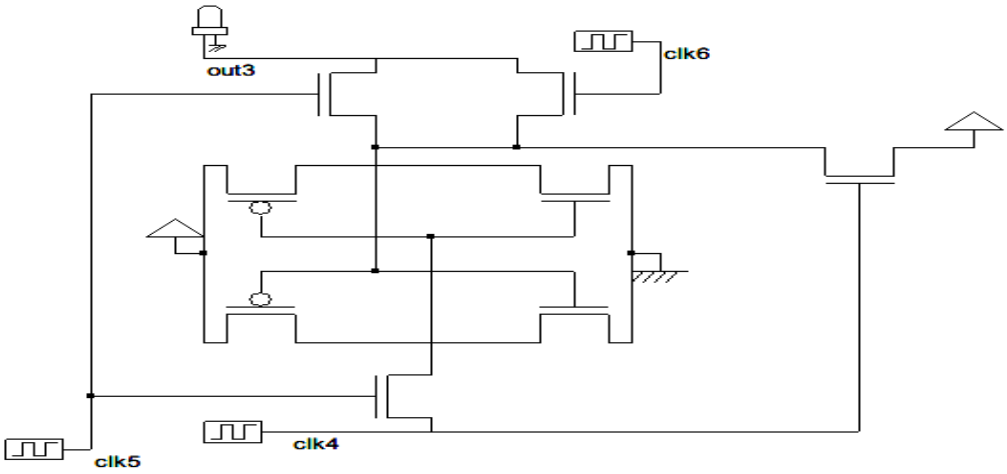

Fig. 4: Read error reduced 8T SRAM cell with reduced transistor count

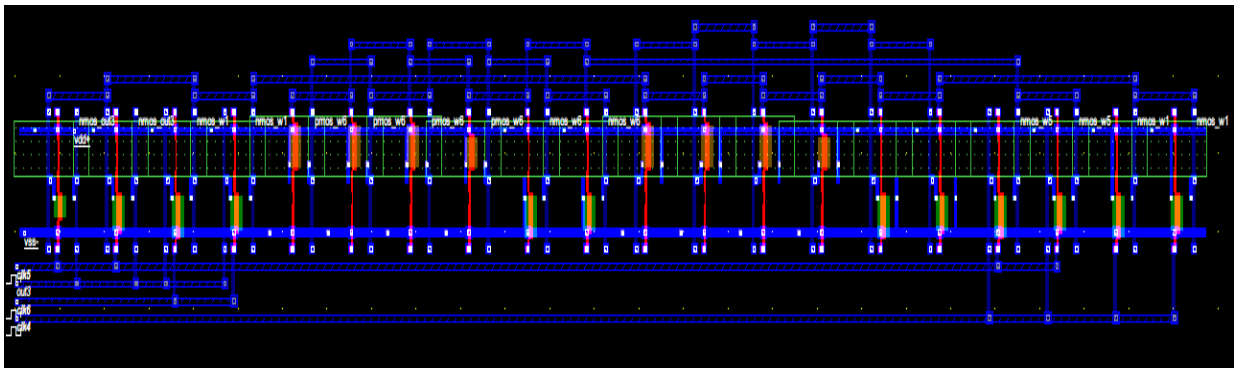

Fig. 5: Layout of 8T SRAM cell with reduced transistor count

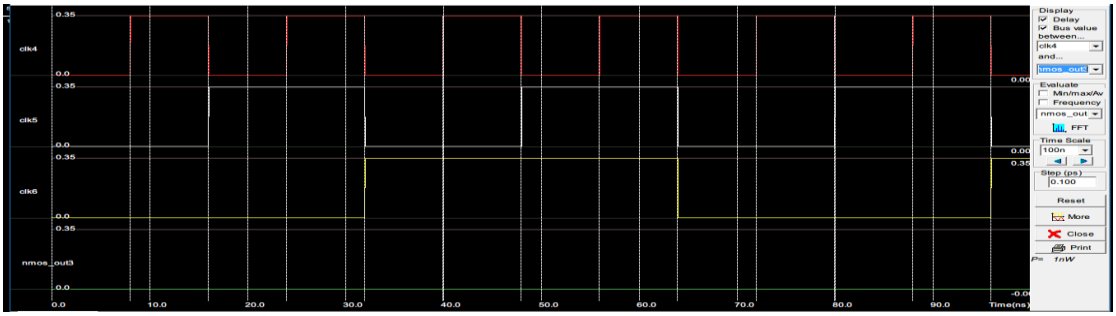

Fig. 6: Voltage Vs Time diagram of 8T SRAM cell with reduced transistor count

Table-1: Performance comparison of ST 1 bit cell with 8T SRAM cell with reduced transistor count

	Power consumed	Area μm^2	memory
ST1 bit cell	2 nW	110.2	6.3
Read error 8T SRAM	1 nW	103.8	5.3

IV. Result Analysis

8T SRAM cell is showing better performance over ST 1 bit cell SRAM in relation to power dissipation area and memory .there is 100 % of improvement in power dissipation in proposed SRAM .Proposed design can be implemented in a lesser area when compared to ST 1 bit cell SRAM.ST 1 bit cell SRAM requires 6.3 % of memory where as proposed design requires only 5.3% of memory

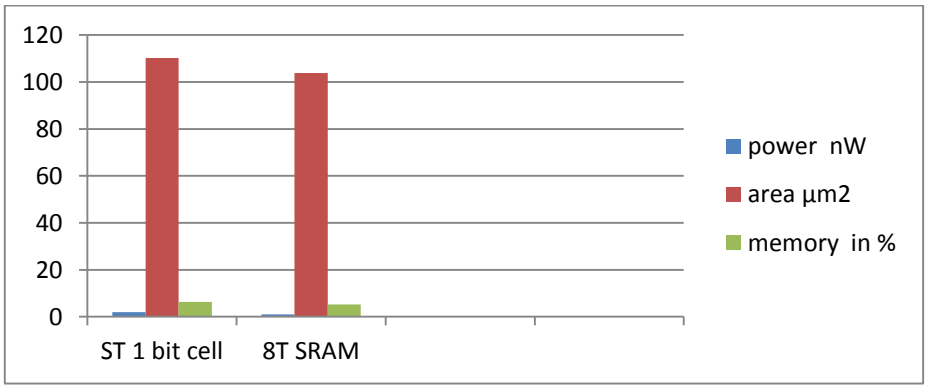

Fig. 7: Power, Area and memory comparison of ST 1bit cell and 8T SRAMs

V. Conclusion

Proposed SRAM design dissipates only 1 nW of power .In proposed design layout combined with 6T & Virtual grounding with read error reduction Circuit concept 32nm technology. And it is having much reduced area than the conventional SRAM designs. Thus this design can be used for future SRAM core memories and Future Integrated circuits for low power and high speed applications using power gated circuits.

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