Design of low power Digital LDO Regulator with Self Clocking Burst Logic

Sorapalli Sharanesh,
Department of Electronics and Communication Engineering,
RV College of Engineering
Bengaluru, India
sharanesh31@gmail.com

Praveen S, Assistant Professor,
Department of Electronics and Communication Engineering,
RV College of Engineering
Bengaluru, India
praveens@rvce.edu.in

***Abstract*—This paper proposes a Digital Low drop-out (LDO) regulator operates in three modes namely burst, normal and sleep modes, to reduce the power while operating a LDO. In this proposed DLDO the output voltage is regulated using two loops when the undershoot/overshoot is detected which are coarse tuning loop and fine tuning loop, the coarse tuning loop uses high frequency clock by compromising with the current efficiency to achieve faster load transient response, this mode is called as burst mode. Later the fine tuning loop uses the low frequency clock by compromising with the speed and by turning off the coarse tuning loop and adjusts the output voltage finely, this mode is called as normal mode. After the voltage is completely regulated D-LDO will set in to sleep mode. The proposed D-LDO is implemented in 18nm fin-FET CMOS technology.**

Keywords*—Low dropout regulator (LDO), digital control, fast transient, coarse fine tuning (CFT), burst-mode, dynamic voltage scaling (DVS), Self generated clock.

I. INTRODUCTION

With the rapid growth in the development of system on chip (SoC), its been very challenging to design a good on chip power management system. A portable and the battery powered devices are needed to supply power to various applications, so the power that needed for all these applications should be reduced because of the limited battery capacity. As a result a low power design techniques and low voltage circuit operations are used to increase power efficiency. So, the sub-threshold or near-threshold logic gates are used to improve the power with the expense of speed.

As shown in the Fig. 1, the LDO is the important block in the power management unit which is follows a DC-DC converter. It is used to regulate the clean voltage supply for different blocks in SoC such as analog, RF, digital circuit blocks. Each LDO regulates a different low voltage domain to each block. The dynamic voltage scaling (DVS) is used to adjust the reference voltage. To minimize the power density different voltages are used for each block depending up on its usage. This increases the number of LDO blocks, so, it is necessary to design a efficient LDO.

The DLDO is first designed in [1]. As shown in the Fig. 2, DLDO consists of digital comparator, bi-directional shift register and PMOS array which is acting as a power transistor. A digital comparator is used to compare the voltage between the reference voltage and output voltage and generates logic 'high' at the output when the V_{out} is higher than the V_{ref} otherwise generates logic 'low'. The signal from the comparator is fed to the shift register to shift right or left and these registers are used to turn on or turn off the PMOS array, thus V_{out} will be varied and brings V_{out} equal to V_{ref}. The comparator will be operated at the sampling frequency. Higher the sampling frequency faster the response.

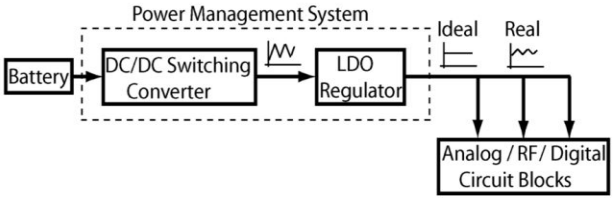


Fig. 1. Block diagram of Power management system

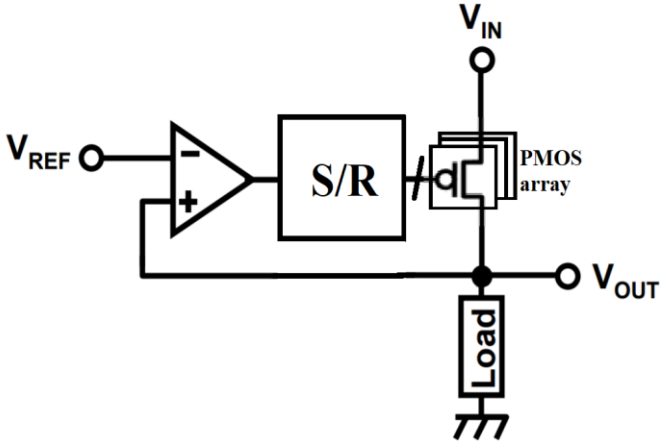


Fig. 2. Block diagram of Power management system

In [2], both PMOS and NMOS arrays are used as the power transistor, after a overshoot or a undershoot has occurred, PMOS arrays are operated at the beginning for the coarse tuning and later NMOS arrays are operated for the fine tuning to increase the power efficiency. In [3], a voltage controlled delay line (VCDL) and phase frequency detector (PFD) is used to compare the V_{out} and V_{ref} voltages and designed a LDO for faster response. A flash ADC is used to compare the the voltages for the higher transient response than the error amplifier [4]. In [5], after overshoot or undershoot LDO selects the burst mode and operates at high Frequency with coarse tuning and later LDO selects the normal mode and operates at low frequency for fine tuning. In [6], during the burst mode a high clock will be self generated and LDO will operated during normal mode low

frequency is used same as [5], when the output voltage is equal to the reference voltage the LDO will switches to sleep mode by turning off some of the blocks to save power. Asynchronous DLDO regulators are designed in [7] and [8] by which the latency of DLDO is reduced in control loop and transient response is improved.

II. PROPOSED DLDO

A. *Operations of PMOS loops*

The PMOS block in the design are divided into two parts coarse and fine, the coarse section draws current N times than of the fine section. Both the PMOS blocks are controlled by the two independent counters, each register of the counter indicates the respective PMOS to be turned on or turned off.

When overshoot or undershoot is occurred and the voltage is crossed the boundaries $V_{ref\text{-}L}$ or $V_{ref\text{-}H}$ then the coarse PMOS power transistor loop are operated at the burst mode with high clock frequency and the counter counts each bit in each cycle and PMOS are operated with the high speed and output voltage will be regulated with the high speed. So, the high quiescent current will be drawn, but this high quiescent will lead to high power consumption.

To overcome this issue the fine PMOS loop has been introduced. When the V_{out} is in between $V_{ref\text{-}L}$ or $V_{ref\text{-}H}$ then the coarse PMOS loop will tuned off and fine PMOS loop will get activated this mode of the operation is called as normal mode, it works with low clock frequency in which the low quiescent current will be drawn and output voltage will be regulated slowly and finely with the lower frequency until the output voltage is brought very much near to the V_{ref}, then the fine PMOS loop also turned off to save the power this mode of operation is called sleep mode.

B. *Architecture*

The overall architecture of a DLDO is shown in Fig. 3. As discussed in the above section, The PMOS array block divided in to two blocks coarse and fine PMOS blocks which are driven by the two independent counters. These counters are controlled by the comparator (comp-1) and the clock controller, comp-1 compares the difference between V_{ref} and V_{out}, and send the difference to the clock controller which operates either of the PMOS loop, comp-1 has two outputs DN and DP.

The low power digital comparator [9] has been used to compare the reference voltages , the schematic of digital comparator is shown in the Fig. 5. During the negative cycle of the clock the latching circuits will get charged and during the positive cycle the comparator gives the output signal (DN and DP) if $V_{ref} > V_{out}$ the comparator generates the output {DN,DP}=01; if $V_{out} > V_{ref}$ the comparator generates the output {DN,DP}=10;

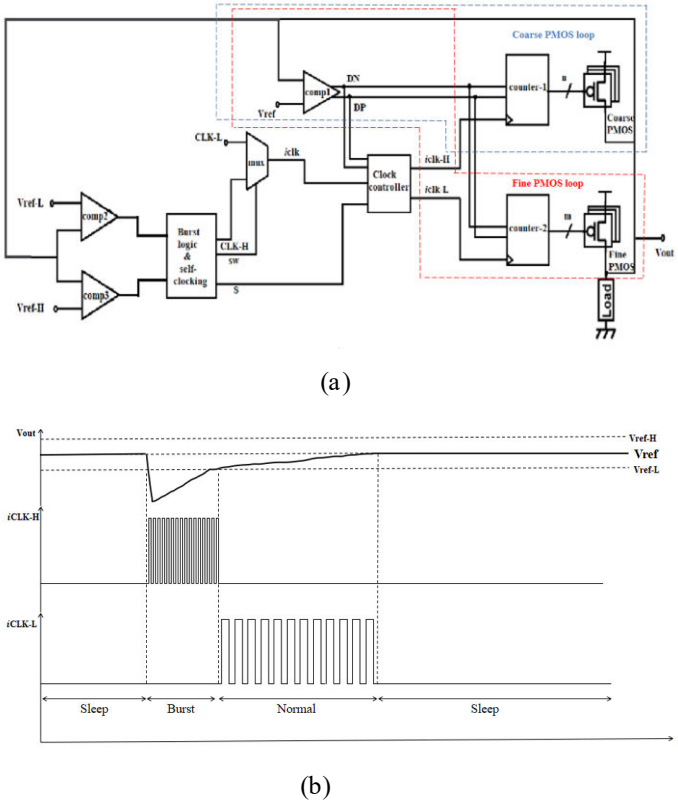


Fig. 3. (a). Block diagram of proposed DLDO regulator (b). Timing diagrams of proposed DLDO regulators

A Synchronous counter has been designed with a control logic to increase or decrease the count, The counter count increases the count if the {DN,DP}=10 or count decreases if the {DN,DP}=01; This count increases or decreases at each cycle with respective to the comparator output. These registers of the counter are used to turn on or turn off the PMOS array. The clock controller takes the input from the comparator and the burst logic controller to select the operating modes (burst mode, normal mode and sleep mode) as discussed in **section 2**.

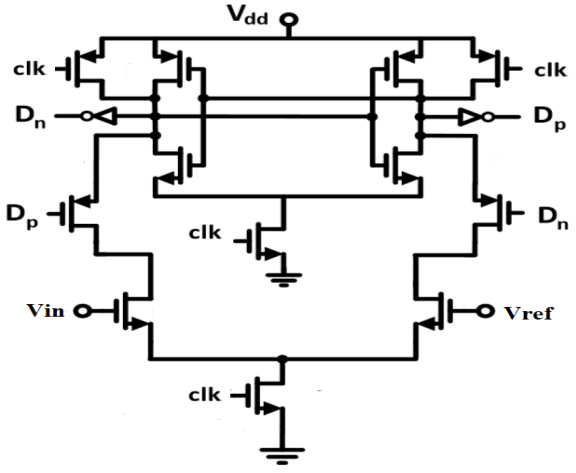


Fig. 4. Digital comparator circuit

The combination of comp-2 and comp-3 will sets the boundries $V_{ref\text{-}L}$ and $V_{ref\text{-}H}$. At the time of overshoot or undershoot, if the output voltage crosses the boundaries then the self clocking circuit will turn on and gives the high clock frequency and burst logic selects the *i*CLK-H using the mux otherwise selects the *i*CLK-L. The Digital controlled oscillator (DCO)[10] circuit is shown in Fig. 5. In which NMOS network is developed to delay the inverter. The input vector (D0, D1 &D2) is given to select the different range of output frequency. This DCO generates the high speed clock CLK-H.

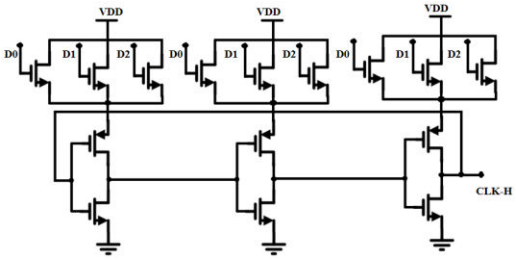
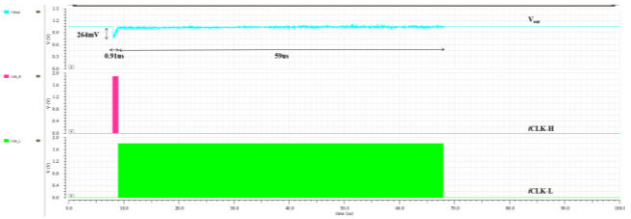


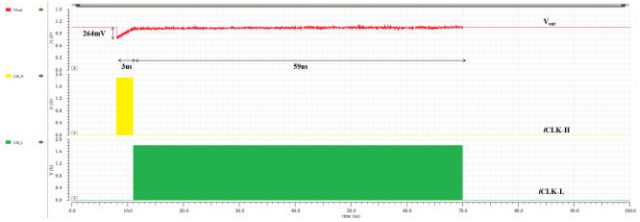
Fig. 5. Digital controlled oscillator circuit

III. Results and Discussion

The proposed DLDO regulator is deigned in 18nm fin-FET technology. The measurement results of the proposed DLDO regulator is shown in the Fig. 6(a). The input voltage of the DLDO is given 1.8V , the reference voltage is set to 1V and the input clock frequency given to the DLDO is 10MHz. The self-clocking block is set to give the high frequency of 1GHz, during the burst mode. The output load is programmed to change the output voltage and the measured undershoot voltage difference is 264mV, the burst mode is activated for 0.91us and output voltage is raised to 0.95V afterwards the normal mode is activated for 59us and the output voltage is set equal to the reference voltage with 0.5% residual error to make the DLDO in sleep mode, the total settling time taken for the output voltage to be equal with the reference voltage is measured as 59.91us.



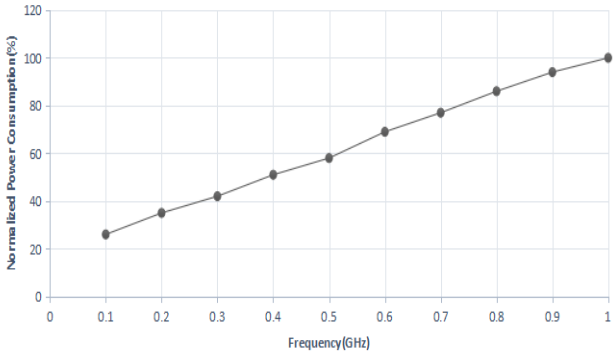
(a)



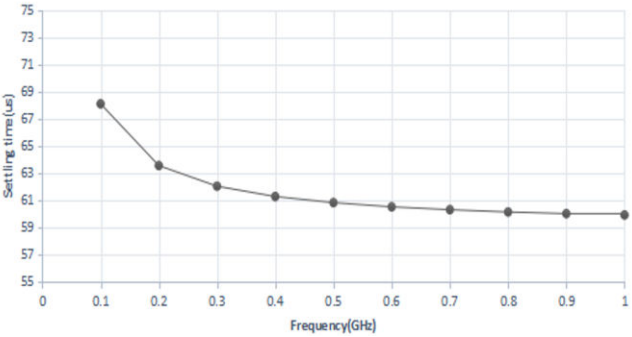
(b)

Fig. 6. Output waveform proposed DLDO regulator with (a). 1GHz high clock frequency. (b). 300MHz high clock frequency

In Fig. 6(b). is shown the transient response of the proposed DLDO regulator where the high clock frequency is reduced to 300MHz, for this condition the burst mode is mode is activated for 3us, and the normal mode is activated same as the above and the total settling time is 62us, but the power consumption of the DLDO is decreased to 58%. Fig. 7(a) shows the normalized power consumption of the proposed DLDO regulator as compared to that of 1GHz frequency with varying high clock frequency. Fig. 7(b) shows the settling time of proposed DLDO regulator with varying high clock frequency.



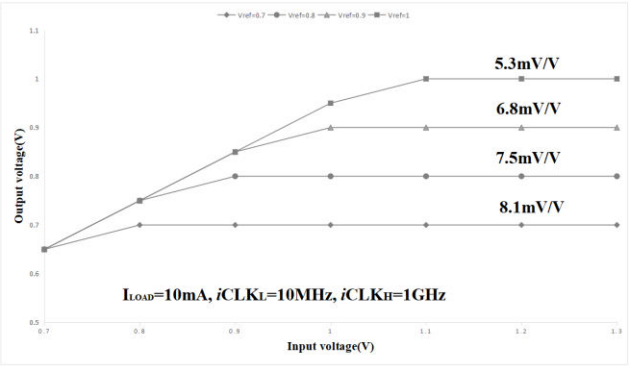
(a)



(b)

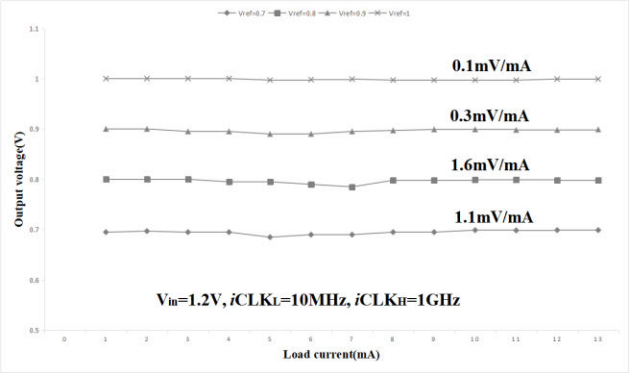
Fig. 7. (a). simulated power power consumption with varying high clock frequency. (b). simulated settling time with varying high clock frequency

Fig. 8(a) shows the V_{out}-V_{in} characteristics of the proposed DLDO regulator at I_{LOAD} of 10mA, the high clock frequency of 1GHz and the low clock frequency of 10MHz. V_{ref} is varied from 0.7V to 1V by 1V step. The measured line regulation is less than 8.1 mV/V.



(a)

Fig. 8(b) shows the V_{out}- I_{LOAD} characteristics of the proposed DLDO regulator at V_{in} of 1.2V, the high clock frequency of 1GHz and the low clock frequency of 10MHz. V_{ref} is varied from 0.7V to 1V by 1V step. The measured load regulation is less than 1.6 mV/V.



(b)

Fig. 8. Measured DC regulation of the proposed DLDO regulator (a)Line regulation. (b)Load regulation

IV. CONCLUSION

The DLDO with self clocking burst logic is designed in 18nm Fin-FET technology to recover the output when the overshoot or undershoot occurred due to the transient response voltage. The coarse and fine PMOS loops of DLDO is operated in burst and normal mode respectively by turning off the certain blocks of the DLDO. Sleep mode is used to save the power after the output voltage is set equal to the reference voltage by turning off all the blocks except comparator. The power consumption reduces if the frequency of the self-clocking block is reduced with the degradation of the speed. The maximum frequency that can be operated in the proposed design is 1GHz.

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